The ATLAS Tracker Upgrade.

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Autumn Block Course 2011
DESY Zeuthen

Thanks to: Marzio Nessi, Tony Affolder, Phil Allport, Nigel Hessey, Peter Vankov, Christoph Rembser, ….

Overview

I. Introduction

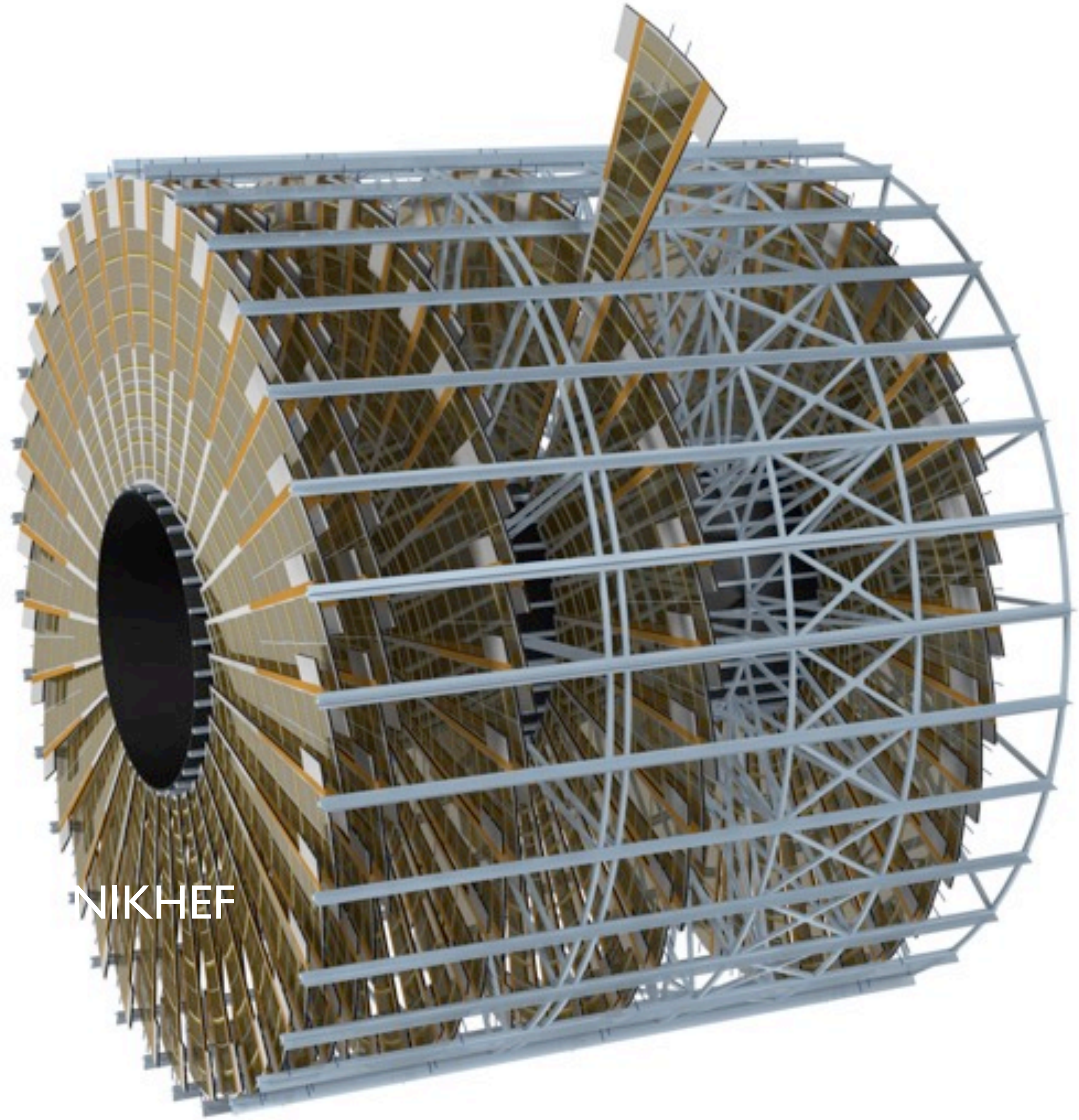
II. LHC Upgrade

III. Phase 0 Upgrade

- The IBL

IV. Phase 2 Upgrade

V. Conclusion

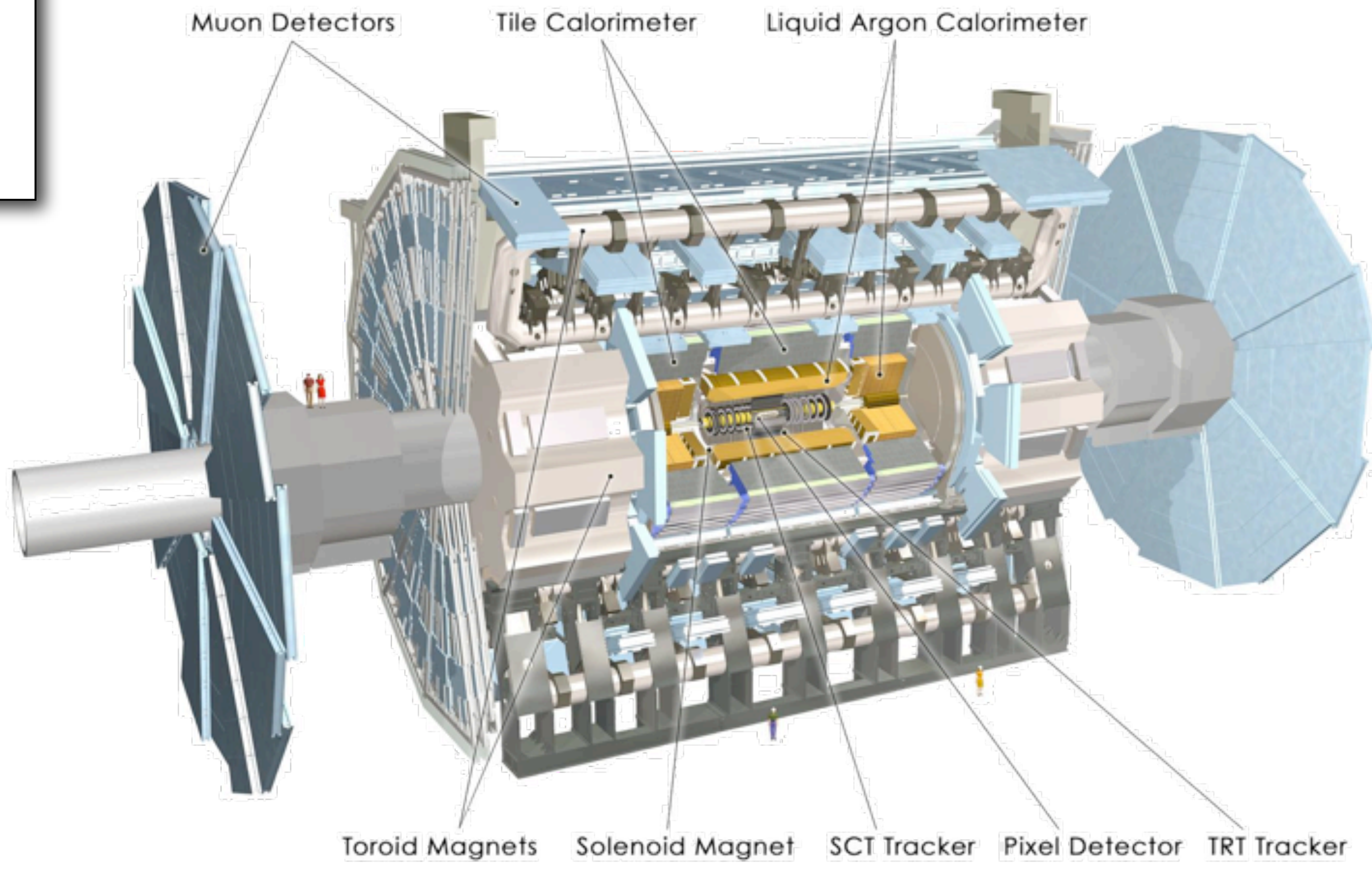


Introduction

The ATLAS Detector

3 Level Trigger system

- L1 – hardware – 100 kHz
  2.5 μs latency
- L2 – software – 3-4 kHz
  10 ms latency
- EF – software – 100 Hz
  1-2 s latency



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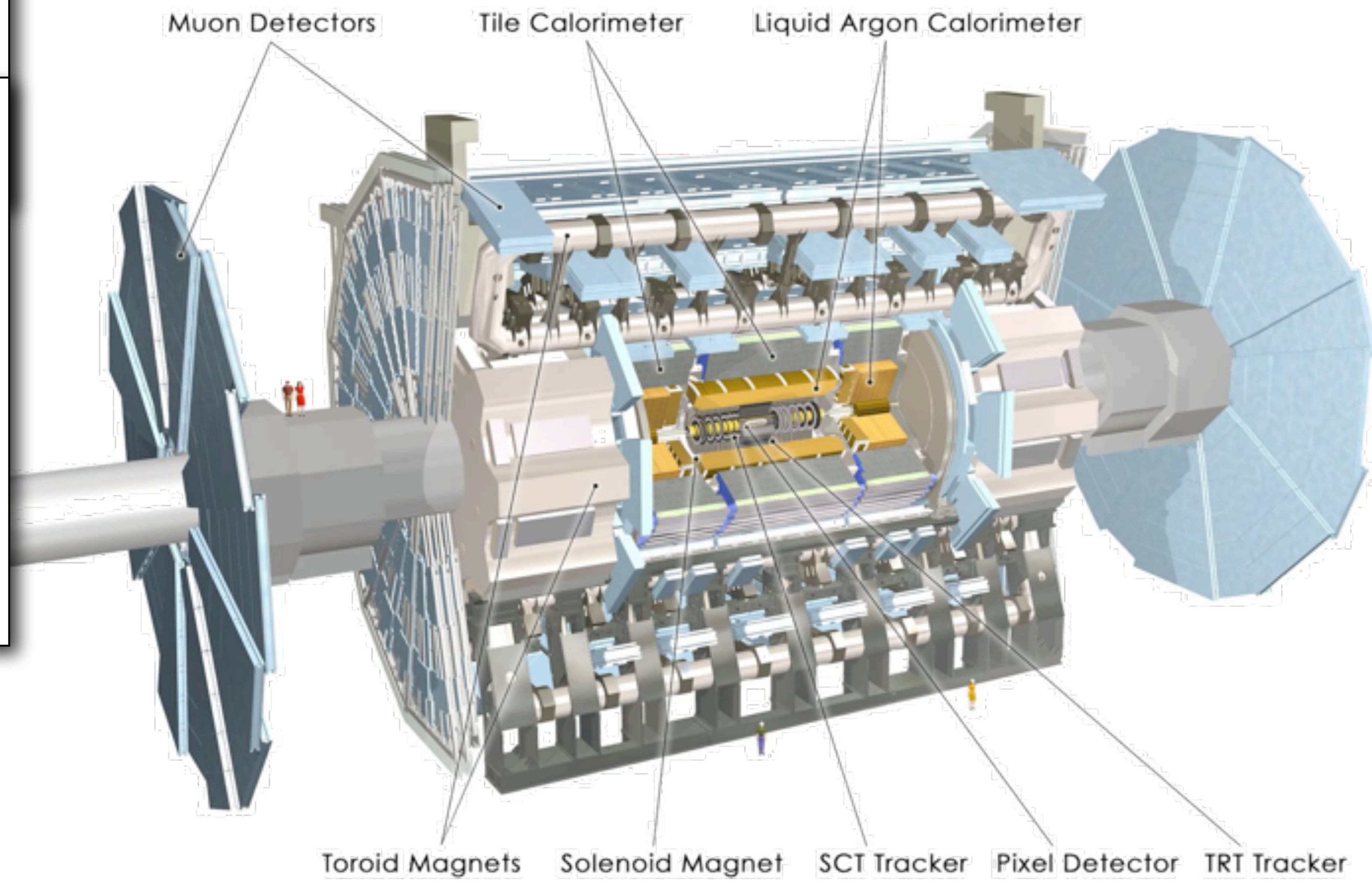
Muon spectrometer
μ tracking

- MDT (Monitored drift tubes)
- CSC (Cathode Strip Chambers)
- RPC (Resistive Plate Chamber) Trigger
- TGC (Thin Gas Chamber) Trigger
- 4T Toroid Magnet



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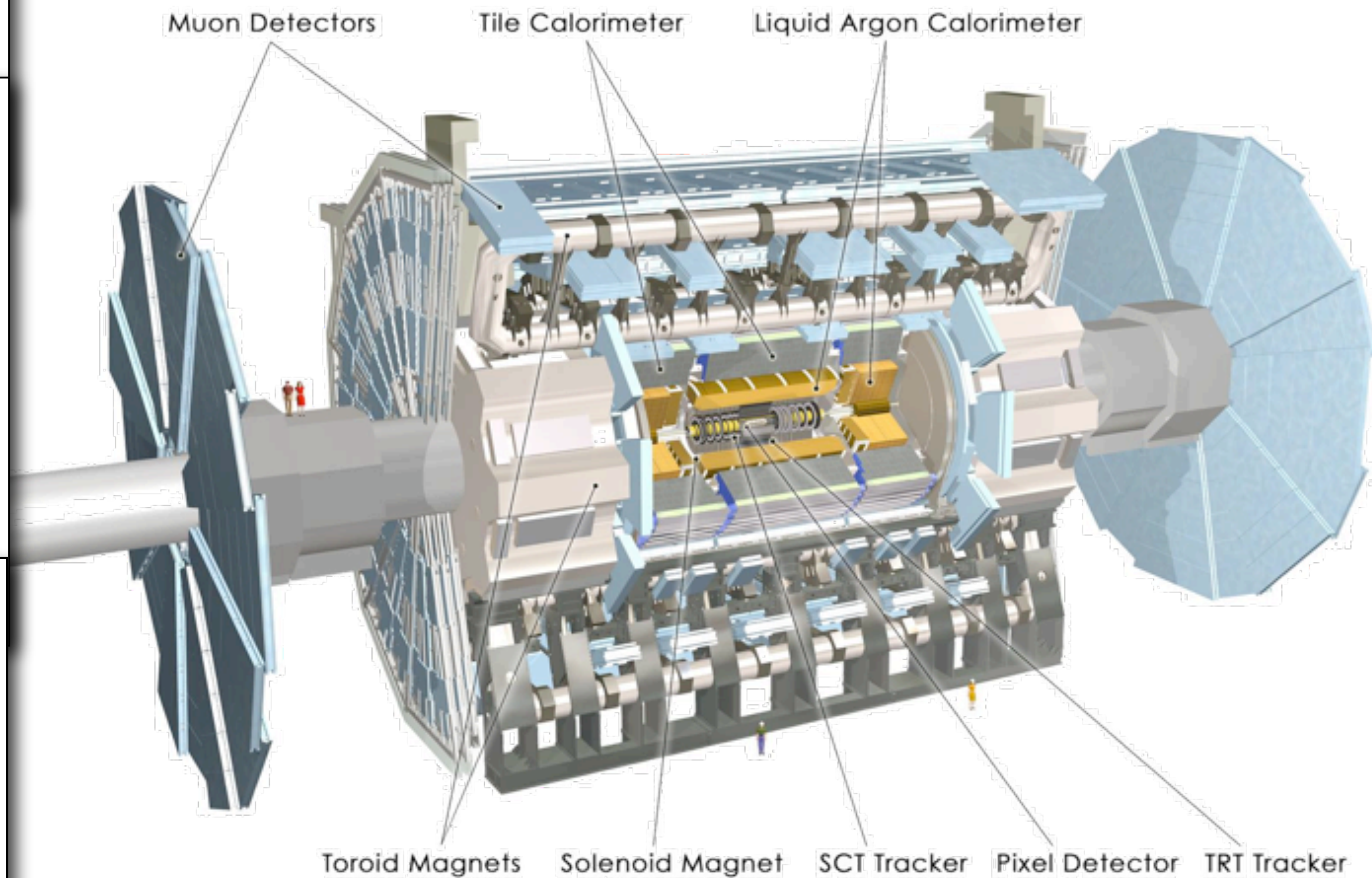
Calorimeter system
EM and Hadronic energy

- Liquid Ar (LAr) EM barrel and end-cap
- LAr Hadronic end-cap
- Tile calorimeter (Fe – scintillator) hadronic barrel



The ATLAS Detector

3 Level Trigger system

- L1 – hardware – 100 kHz 2.5 μs latency
- L2 – software

Inner Detector (ID) Tracking

- Silicon Pixels 50 x 400 μm^2
- Silicon Strips (SCT) 80 μm stereo
- Transition Radiation Tracker (TRT) up to 36 points/track
- 2T Solenoid Magnet

Muon spectron μ tracking

- MDT (Monitore tubes)
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Calorimeter system EM and Hadronic energy

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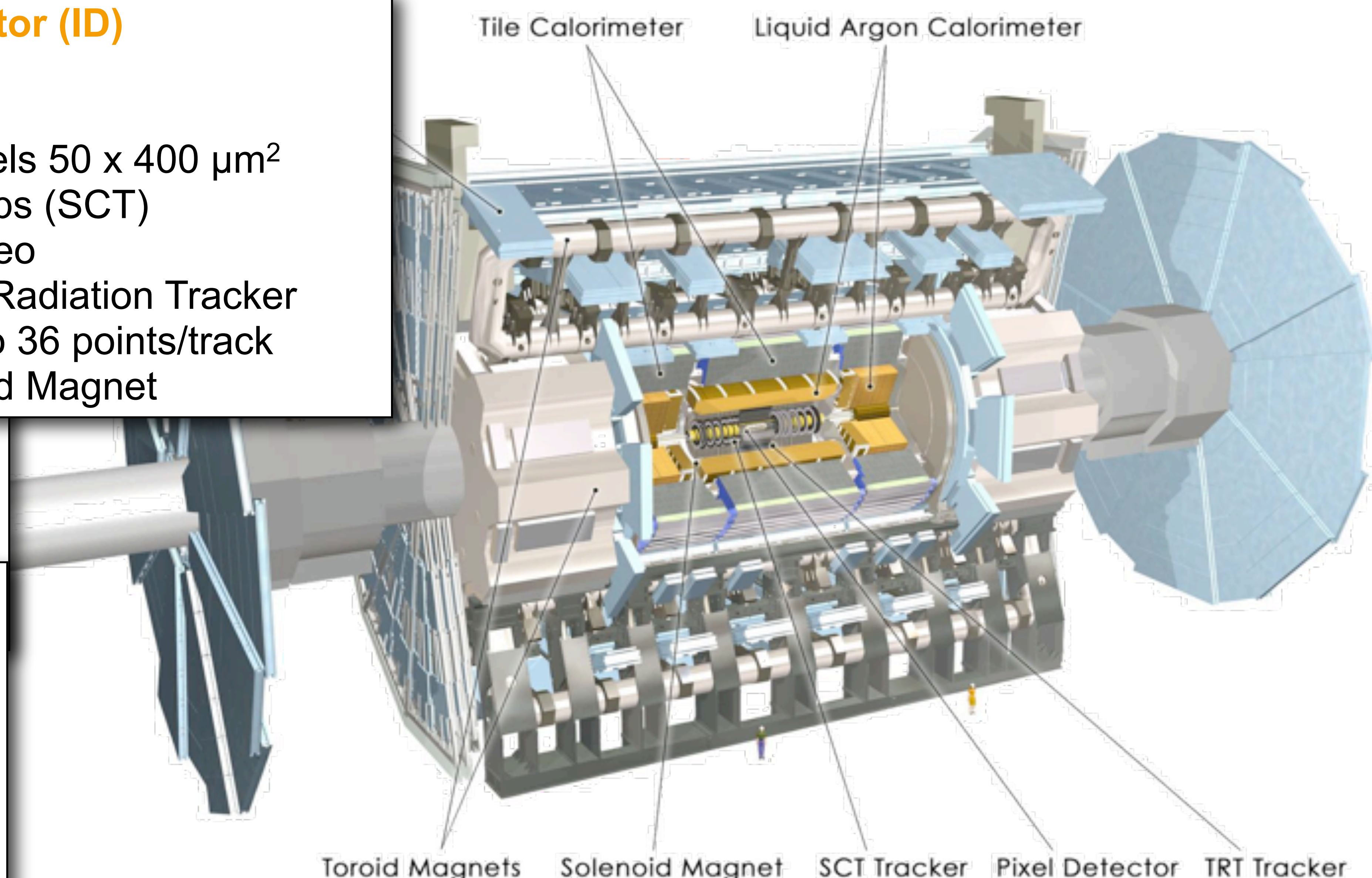
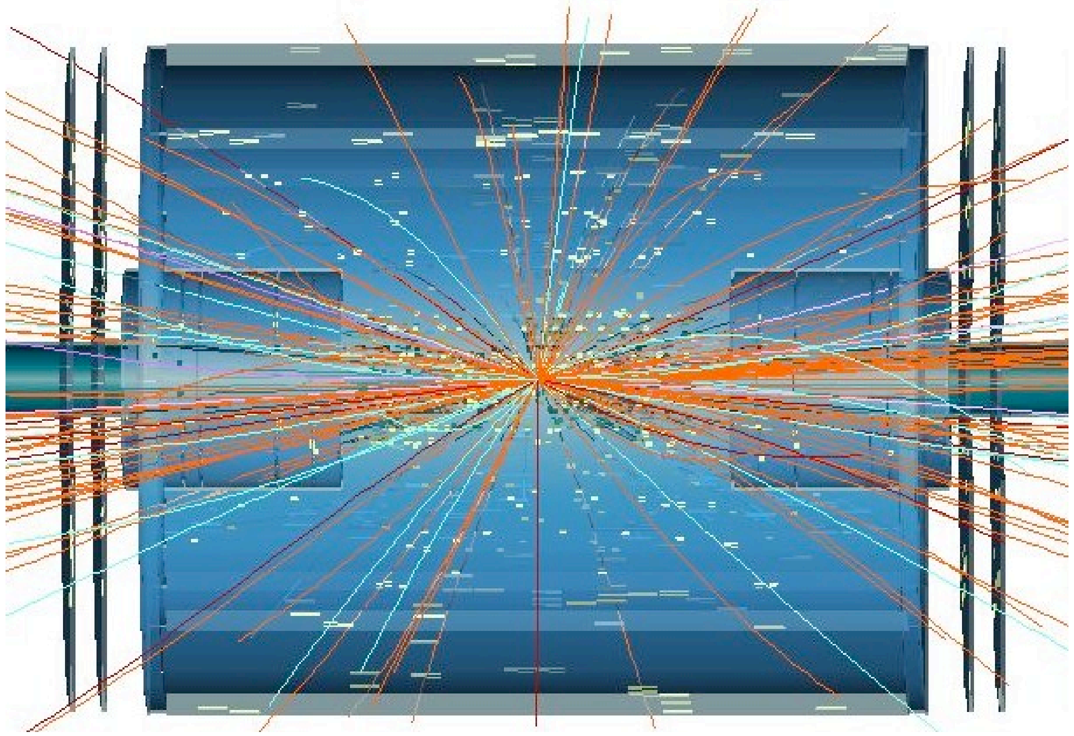
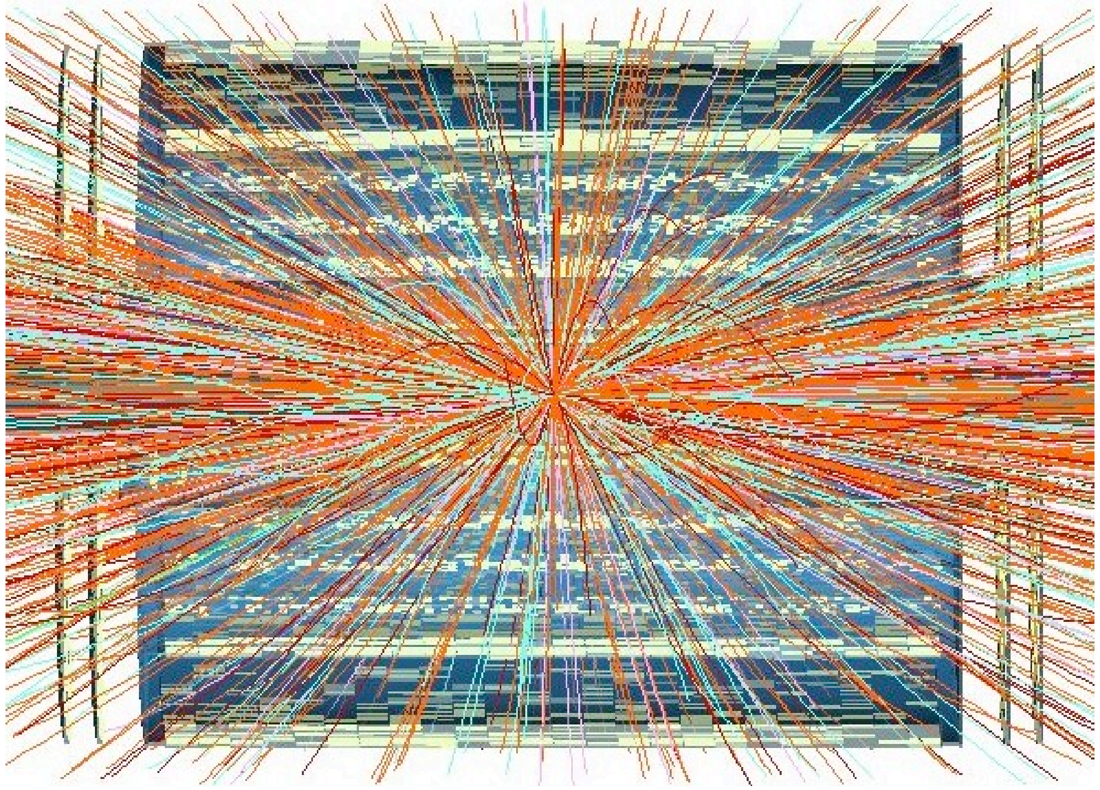


Why Upgrade?

- The new discoveries hoped for will need a lot of data to understand their nature
  - Higgs parameters
  - SUSY – spectroscopy
  - Triple gauge couplings
  - VV scattering at ~1 TeV
- In addition, the potential is significantly extended for (more difficult) physics discoveries

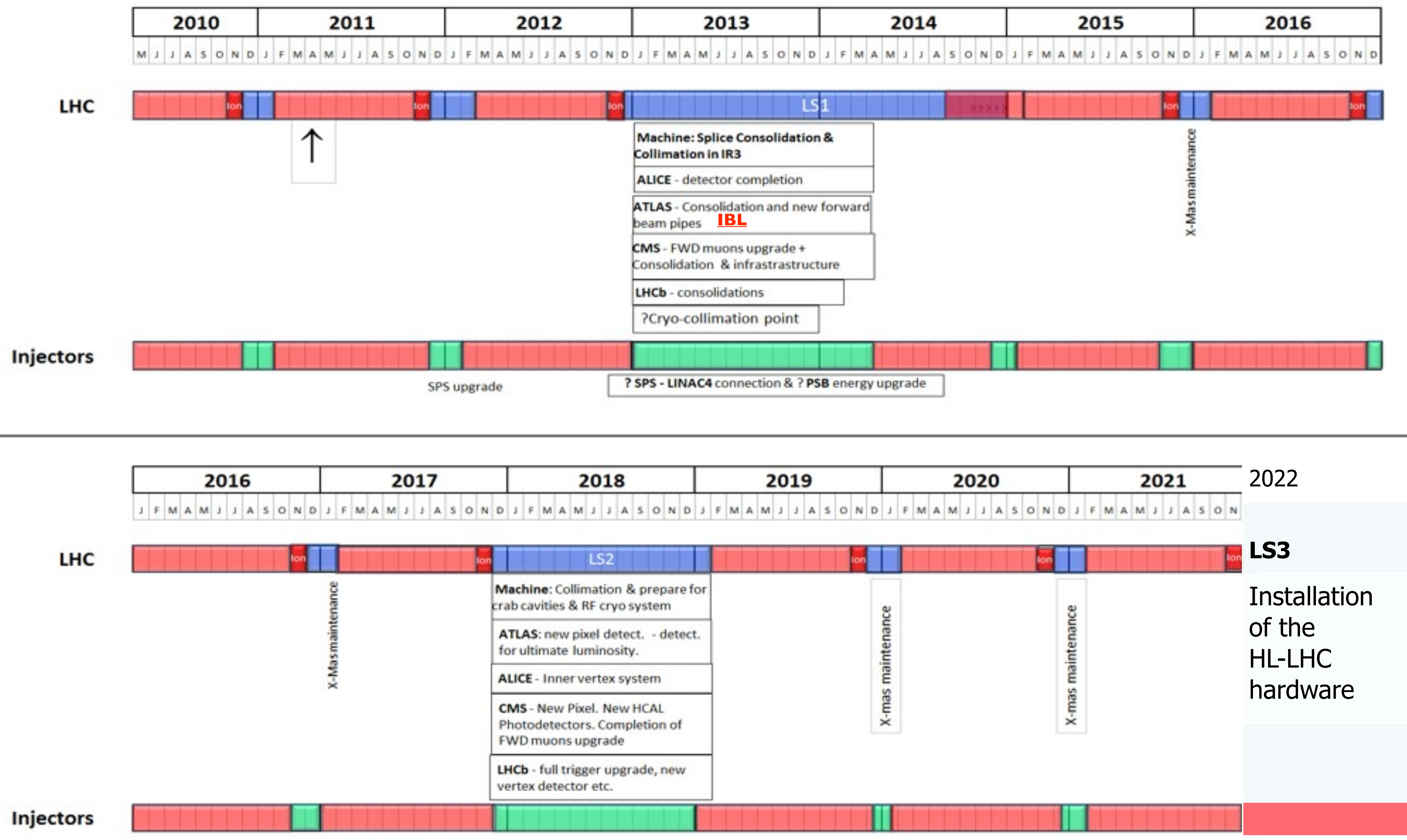


current LHC: 1×10^{33} 1/cm^{2}s



HL-LHC: 5×10^{34} 1/cm^{2}s

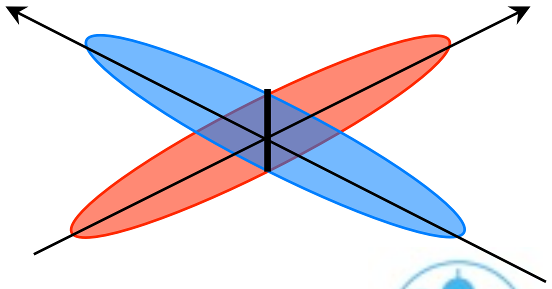
New Rough Schedule for the next 10 years



LHC Machine Upgrade

LHC Upgrade in a Nutshell

$$\mathcal{L} = \left(\frac{\gamma f_{rev}}{4\pi}\right)\frac{n_b N_b}{\beta^\star}\left[\left(\frac{N_b}{\epsilon_N}R_\phi\right)\right]$$



LHC Upgrade in a Nutshell

Total beam current. Limited by:

- Uncontrolled beam loss!!
- E-cloud and other instabilities
- Action: Linac4

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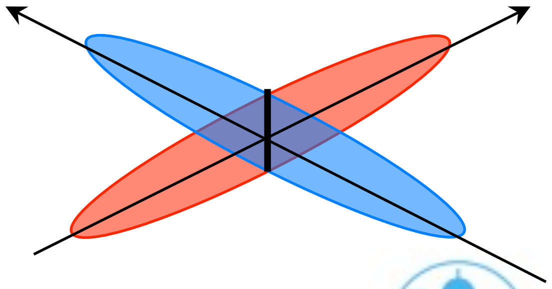

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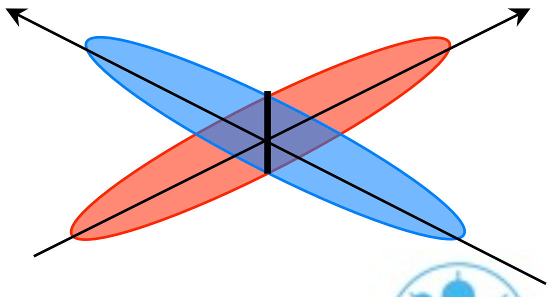
Reduce β*, limited by
- magnet technology -> Nb3Ti
- chromatic effects



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Brightness, limited by
- Injector chain
- Max tune-shift

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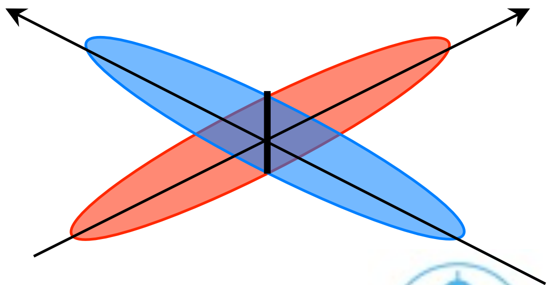

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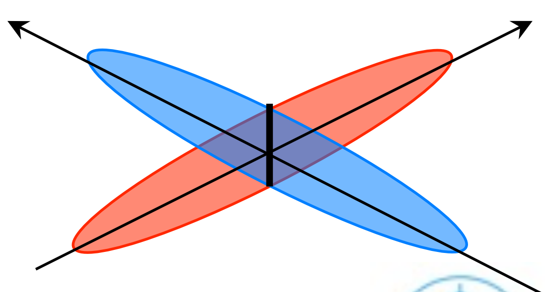
Geometric factor, related to crossing angle and bunch length



LHC Upgrade in a Nutshell

Total beam current. Limited by:
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Maximize number of bunches

Brightness, limited by
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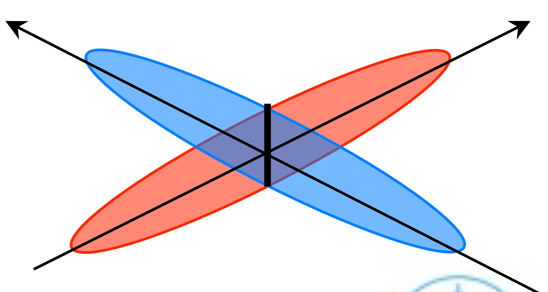
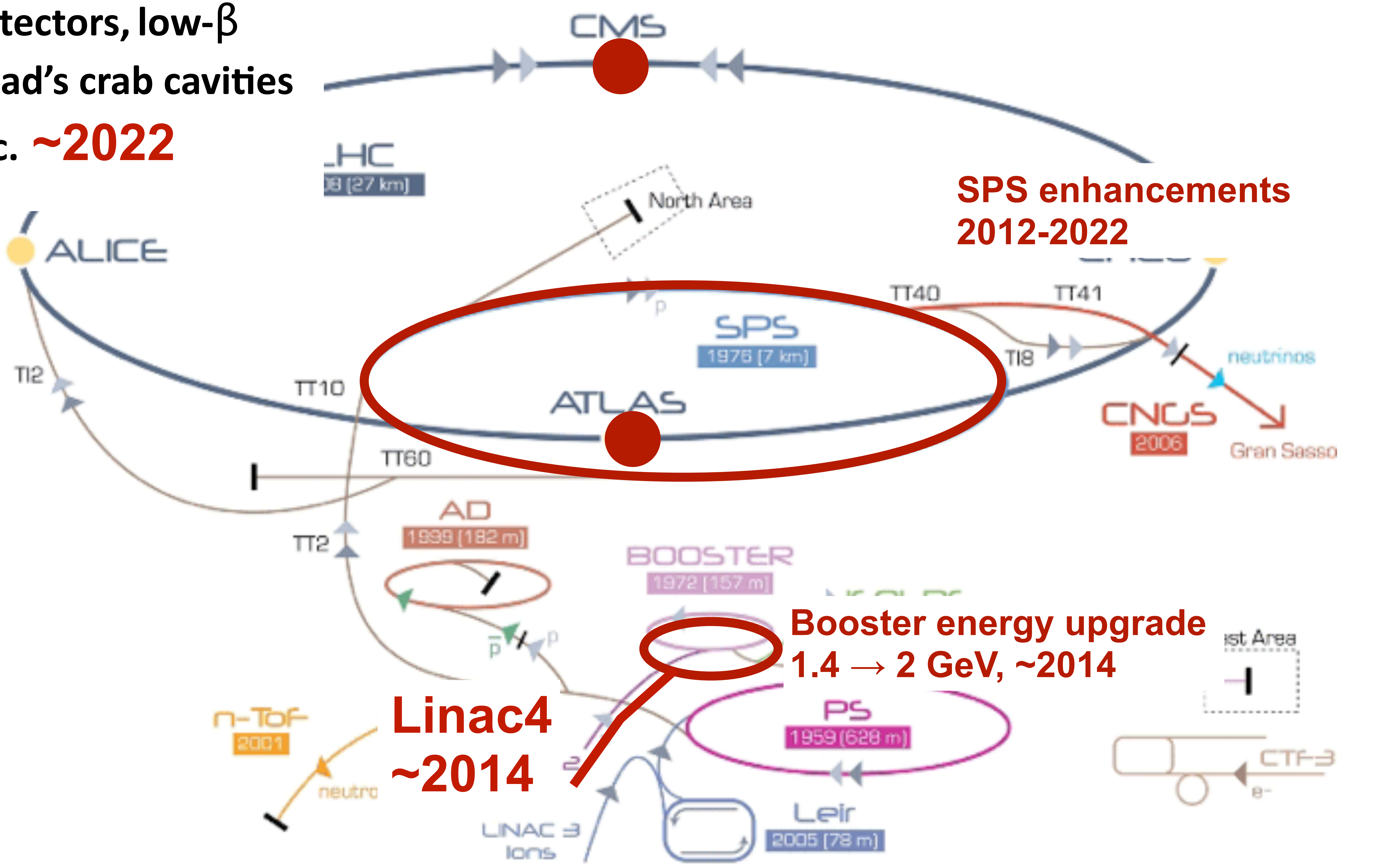


IR Upgrades

detectors, low-β quad's crab cavities etc. ~2022



F. Zimmermann

What can HL-LHC reach ?

Goal:

Leveled peak luminosity: $L = 5\ 10^{34}\ cm^{-2}\ sec^{-1}$

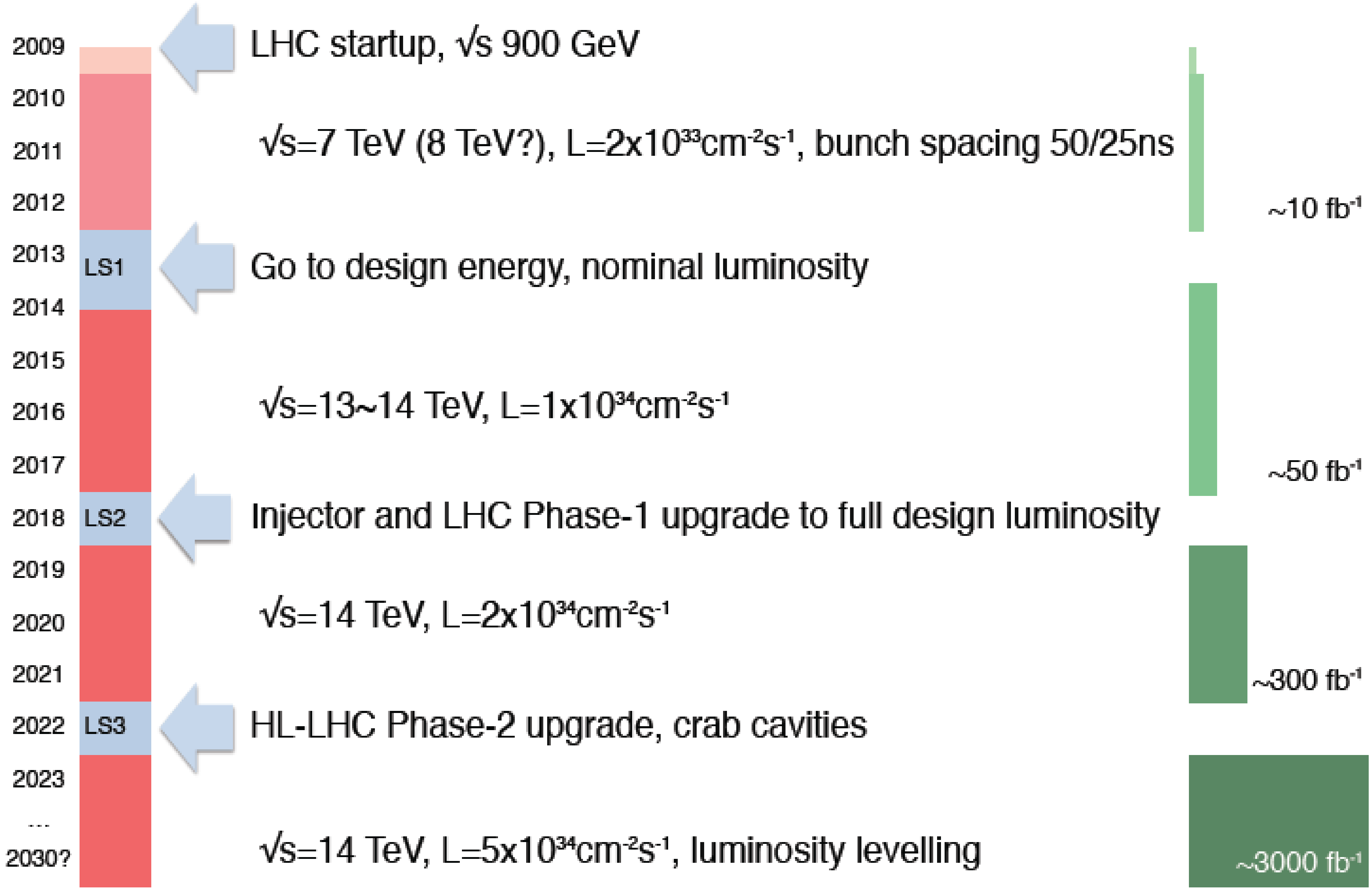
Virtual peak luminosity: $L = 10\ 10^{34}\ cm^{-2}\ sec^{-1}$

Integrated luminosity: $200\ fb^{-1}$ to $300\ fb^{-1}$ per year

Total integrated luminosity: ca. $3000\ fb^{-1}$

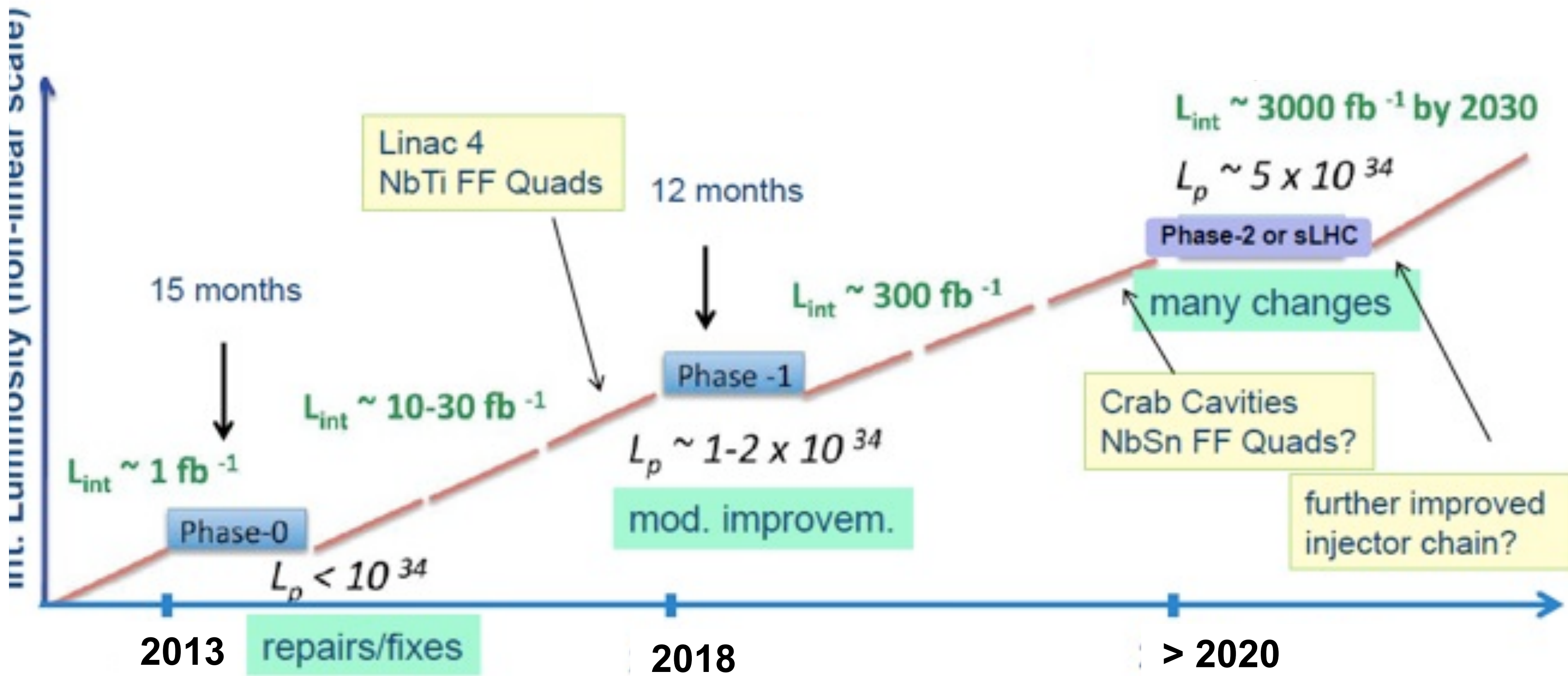
Parameter	nominal	minimum β* 25ns	minimum β* 50ns
N	1.15E+11	2.0E+11	3.3E+11
n_b	2808	2808	1404
beam current [A]	0.58	1.02	0.84
x-ing angle [μrad]	300	475	580
beam separation [σ]	10	10	10
β* [m]	0.55	0.15	0.15
ε_n [μm]	3.75	2.5	3.75
ε_L [eVs]	2.51	2.5	2.5
energy spread	1.00E-04	1.00E-04	1.00E-04
bunch length [m]	7.50E-02	7.50E-02	7.50E-02
IBS horizontal [h]	80 -> 106	25	37
IBS longitudinal [h]	61 -> 60	21	21
Piwinski parameter	0.68	2.5	2.5
geom. reduction	0.83	0.37	0.37
beam-beam / IP	3.10E-03	3.9E-03	3.9E-03
Peak Luminosity	$1\ 10^{34}$	$7.4\ 10^{34}$	$6.8\ 10^{34}$

(Possible) LHC Time-Line



Tentative Schedule and ATLAS Plans

- Phase 0 (2013):
  - **Pixel: Insertable B-Layer (IBL)**
  - Pixel: opto-electronics repair
  - Muon/forward: Beam-pipe -> Beryllium
  - Infrastructure consolidation



- Phase 1 (2018):
  - **NewPix System (under consideration)**
  - Muon: additional SCS layers
  - TDAQ: moderate upgrades, improved level-2 triggers
  - minor consolidations: TRT HV PS, LAr LV PS, ...

- Phase 2 (>2020):
  - **ID: new tracker or only Strip ….**
  - LAr: barrel electronics and new forward elements
  - Tile Calorimeter: new electronics
  - Muons: new forward layers
  - TDAQ: major upgrades

Will concentrate on Phase 0 and Phase 2 -> Phase 1 Tracker Upgrade is still to premature ….

Assumptions on Global Requirements

LHC up to 2021

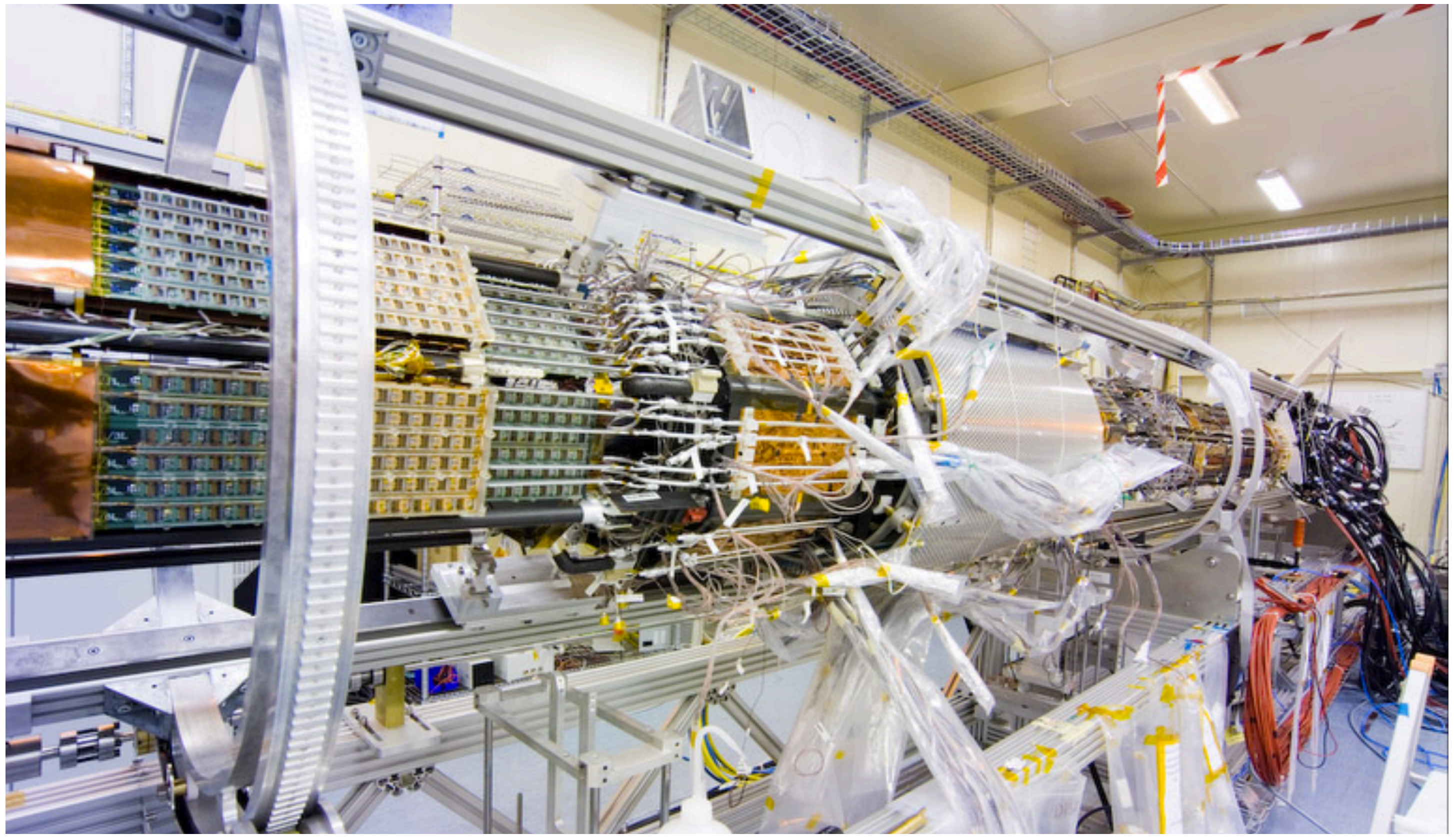
		safer value
Peak Luminosity expected	$2 * 10^{34}$	$3 * 10^{34}$
Integrated Luminosity expected	300 fb^{-1}	400 fb^{-1}
μ = mean number of interactions per crossing	46	69
Safety factor to be used in the dose rate and integrated dose calculations	2	2

HL-LHC after 2022

		safer value
Peak Luminosity expected	$5 * 10^{34}$	$7 * 10^{34}$
Integrated Luminosity expected	2500 fb^{-1}	3000 fb^{-1}
Int. Luminosity per year expected	250 fb^{-1}	300 fb^{-1}
μ = mean number of interactions per crossing	140	200
Safety factor to be used in the dose rate and integrated dose calculations	2	2

Phase 0 Upgrade
(2013/2014 Shutdown LS1)

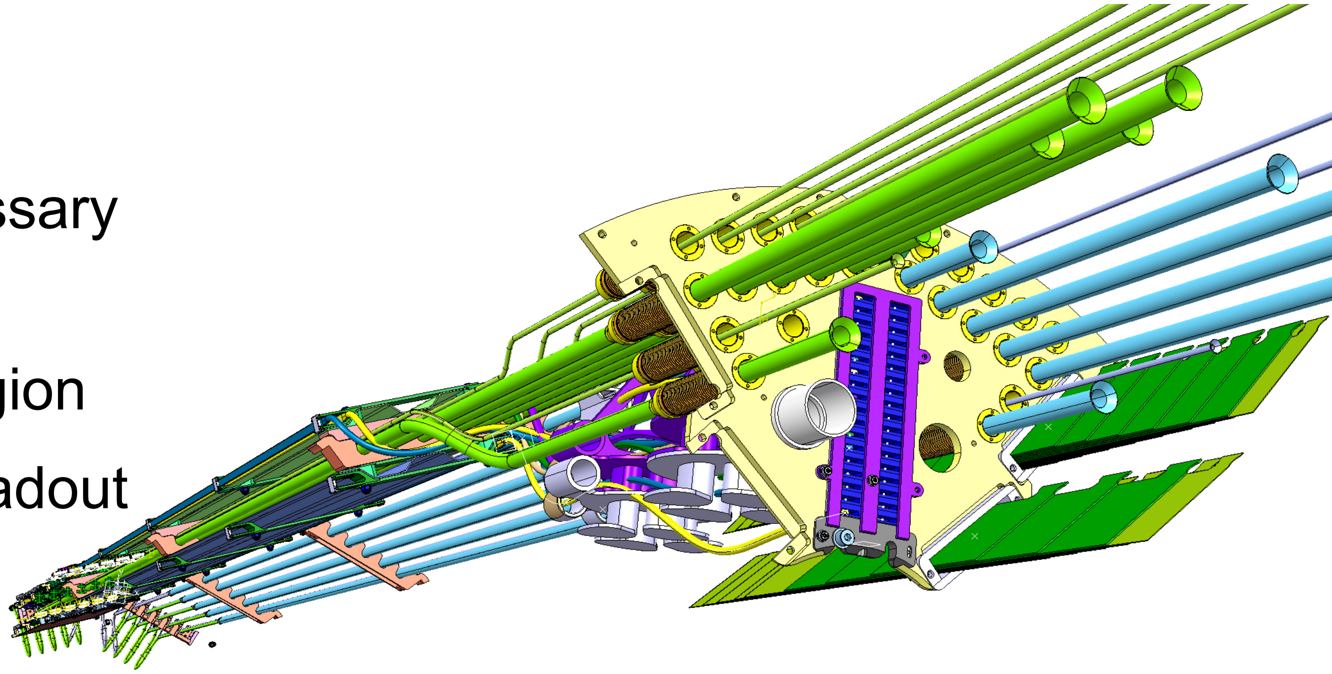
New Service Quater Panel



Be ready to take the final decision if to extract and repair or not the pixel detector on the surface during 2012 (first half)

Plans (work ongoing):

- Rebuild in 2011-12 the readout services necessary on the detector (Service Quarter Panels)
- Bring the optical links in a more accessible region
- Recent: introduce fixes to allow an efficient readout at ultimate Luminosity (double some readout channels,….)



The Insertable B-Layer (IBL)

CERN-LHCC-2010-01

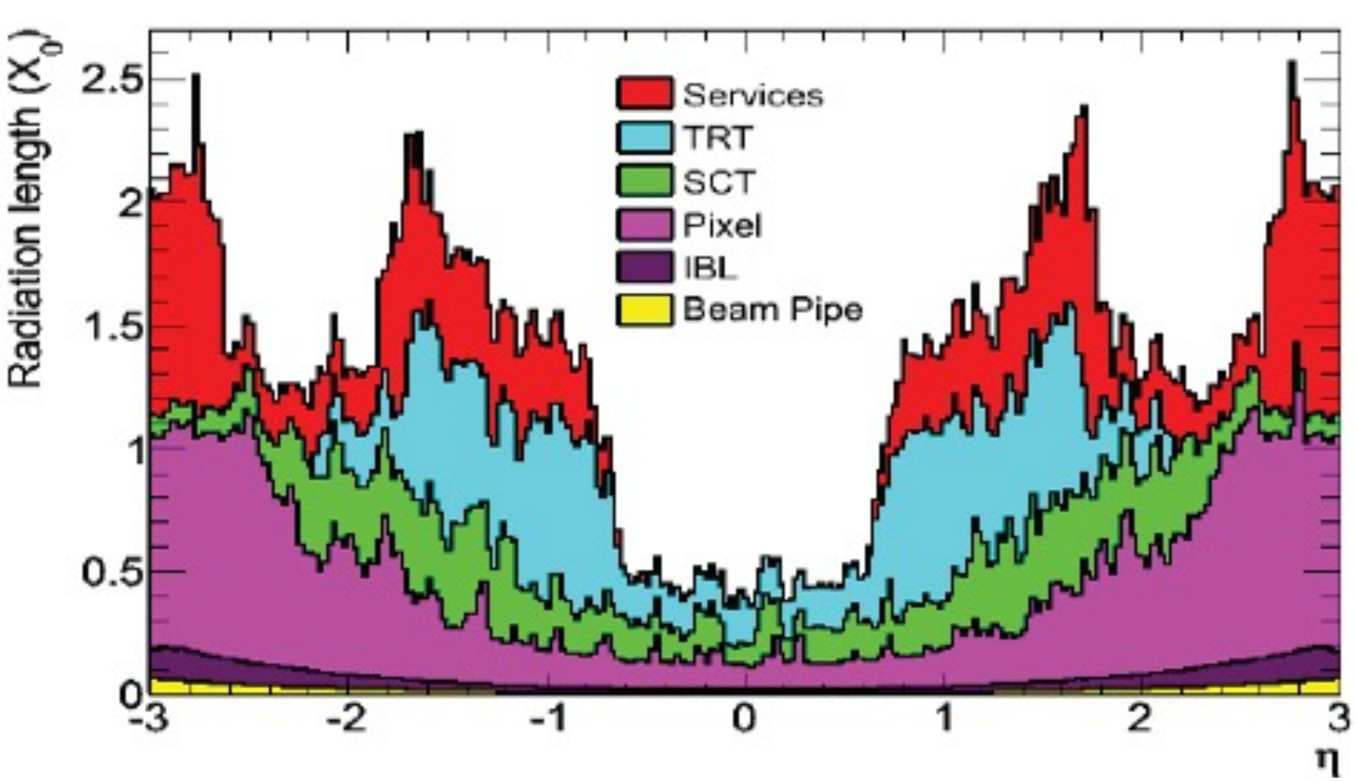
- Excellent vertex detector performance is crucial
  - improvement heavy flavor tagging, primary and secondary vertex reconstruction/separation
- Additional innermost layer will boost tracking performance
  - adds additional redundancy of the detector in case of radiation damage
- Replacement is technically very challenging
  - ATLAS strategy: insert a completely new layer at small radius
  - needs decrease of pipe radius
- New IBL schedule since "Chamonix 2011":
  - All modules installed on staves by end 2012
  - Twice the needed number of sensors by mid 2012
  - Full number of sensors in preproduction till Oct 2011

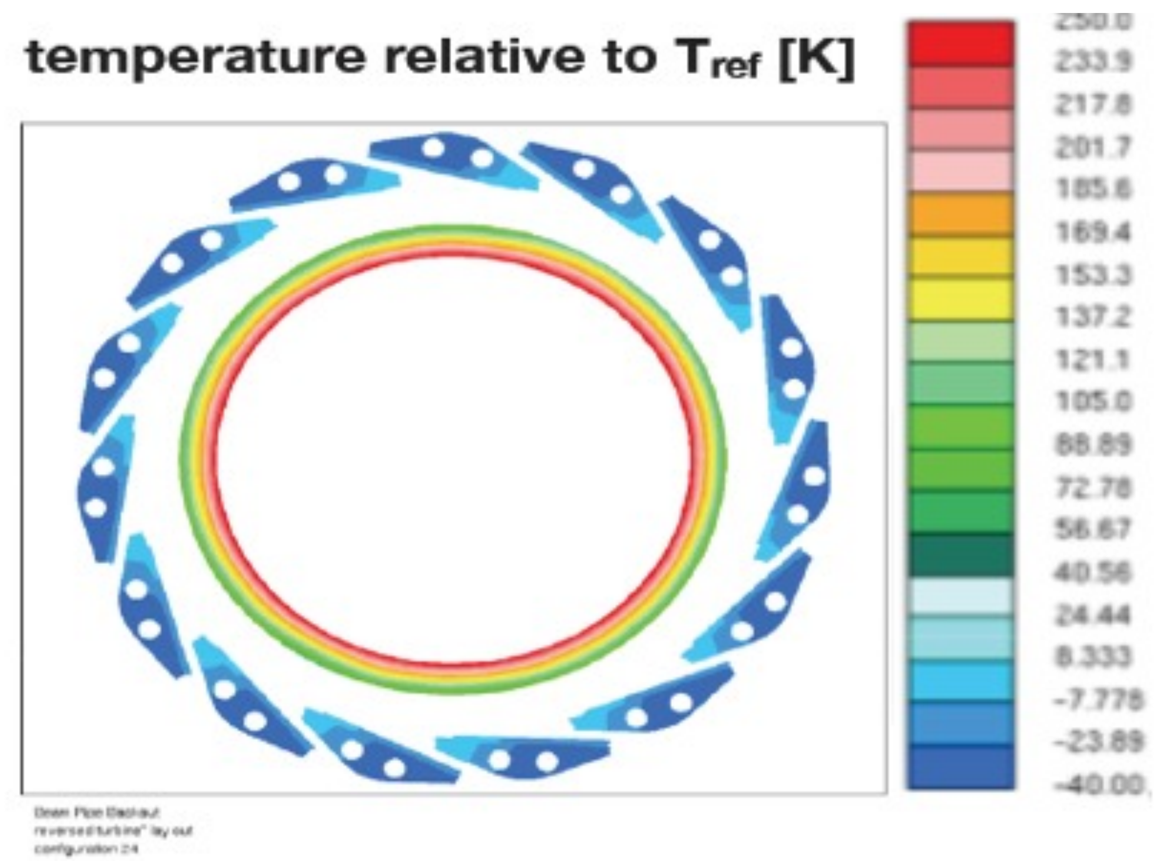
Present Beam Pipe & B-Layer

IBL: A Technological Challenge

- Additional layer inserted increases material budget
  - sensor and support material needs to be minimized
  - the detector has to be powered, read-out and cooled

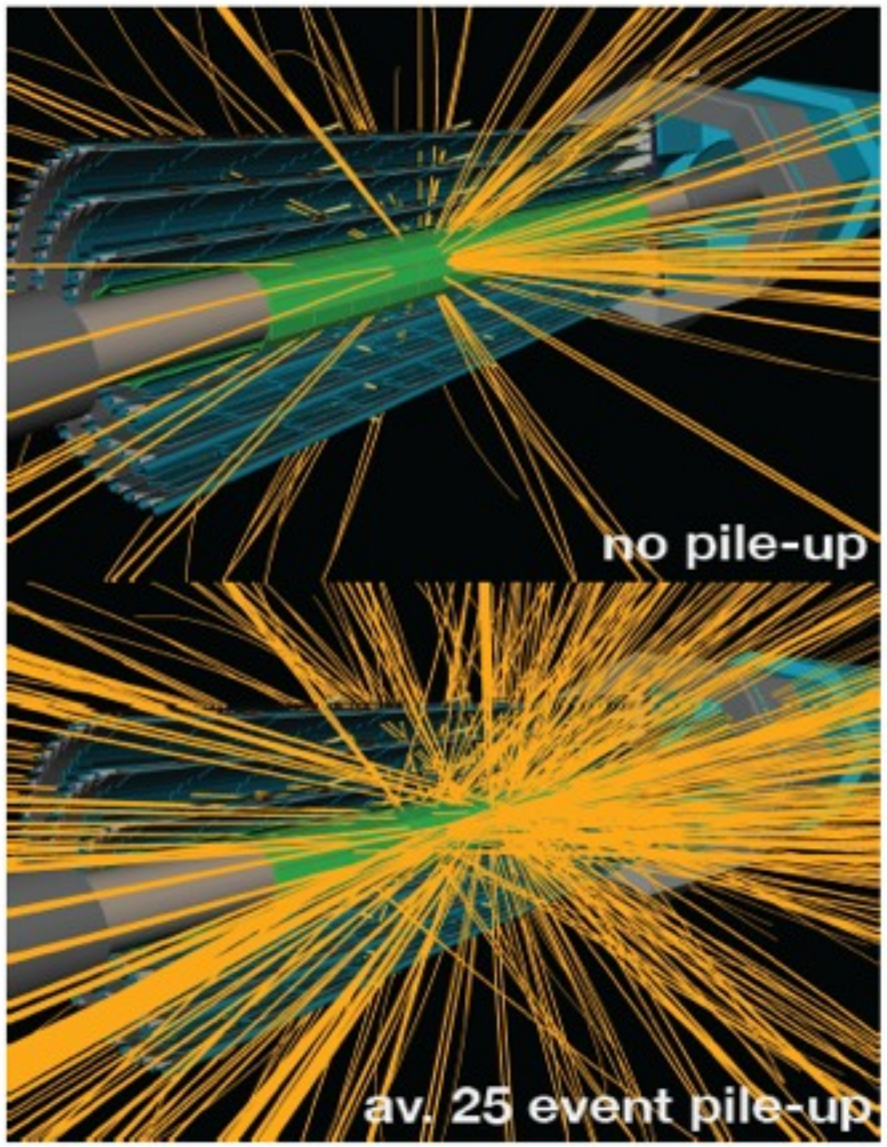
- New stave design in carbon foam structure
  - low material budget, while building excellent heat path to cooling pipe

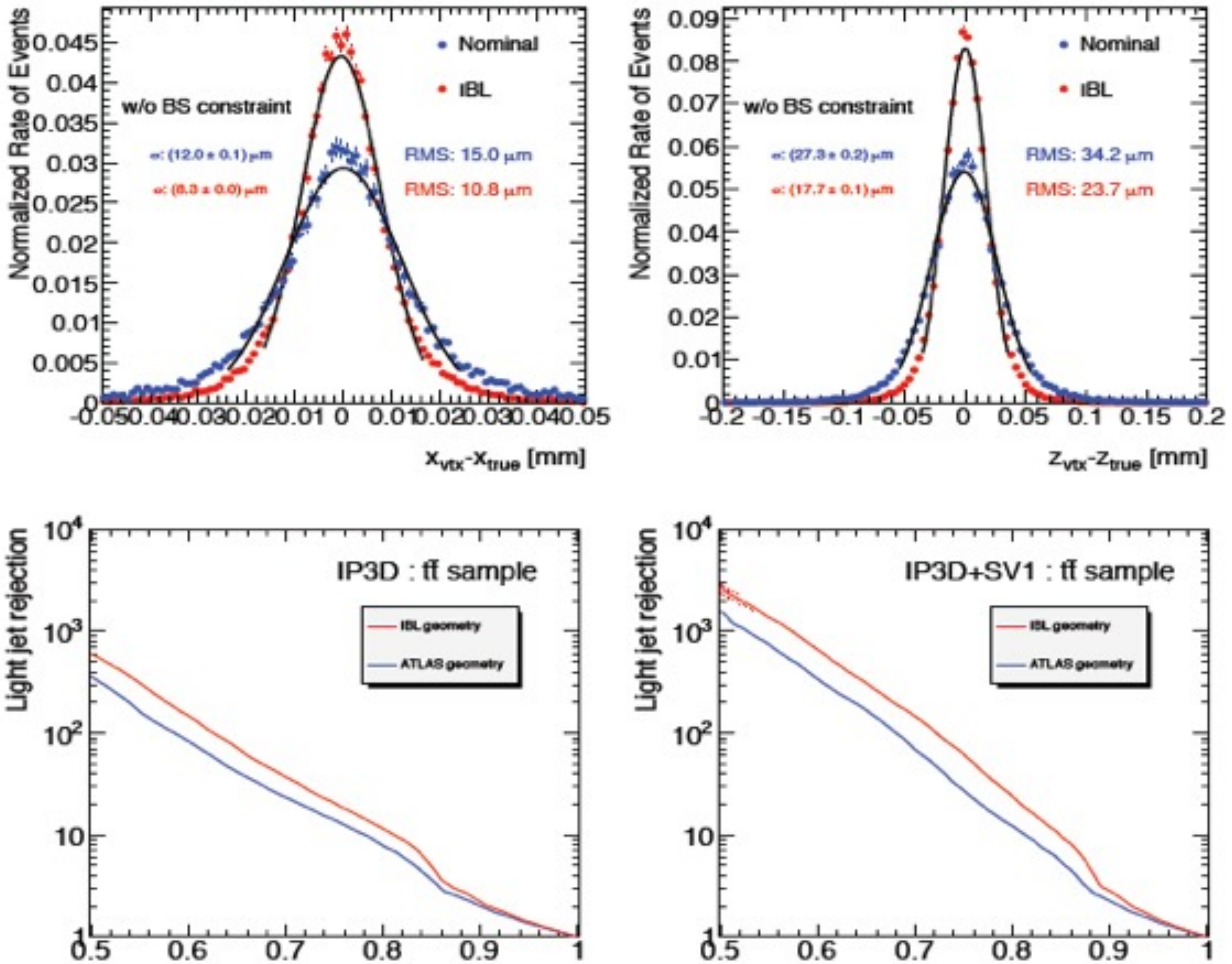




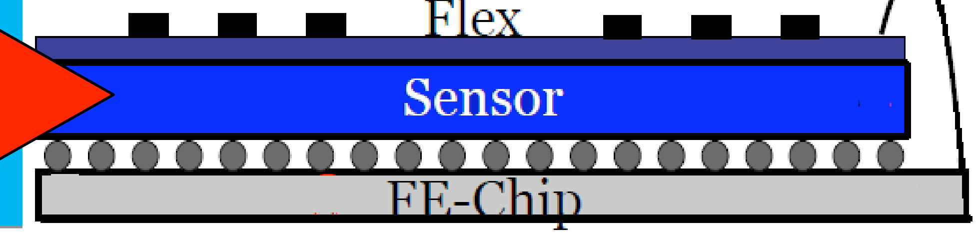
IBL: Performance Improvements

- Simulation shows significant improvements
  - vertex resolution, secondary vertex finding
  - light jet rejection at constant b-tagging efficiency
  - IBL studies needed update of track reconstruction





Three Different Sensor Approaches



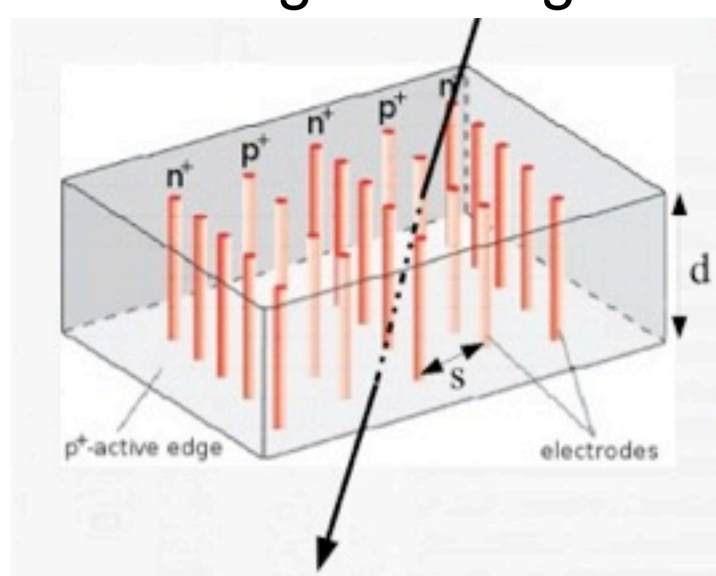
Hybrid Pixel Chip Assembly

Planar Sensor

- current design is an n-in-n planar sensor
- silicon diode
- different designs under study (n-in-n; n-in-p ....)
- radiation hardness proven up to 2.4 . 10^{16} p/cm^2
- problem: HV might need to exceed 1000V

3D Silicon

- Both electrode types are processed inside the detector bulk instead of being implanted on the wafer's surface.
- Max. drift and depletion distance set by electrode spacing
- Reduced collection time and depletion voltage
- Low charge sharing

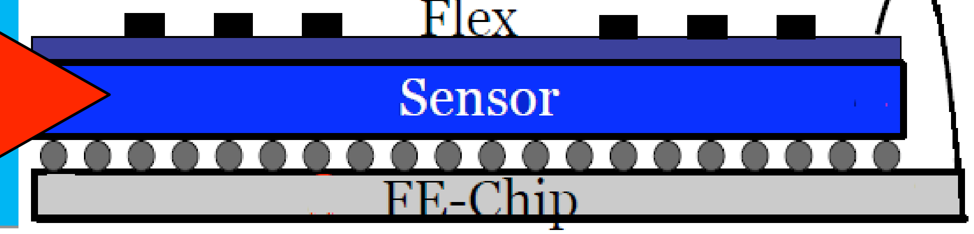


CVD (Diamond)

- Poly crystalline and single crystal
- Low leakage current, low noise, low capacitance
- Radiation hard material
- Operation at room temperature possible
- Drawback: 50% signal compared to silicon for same X_0 , but better S/N ratio (no dark current)

Review in July 2011 to decide which technology to be used for IBL

Three Different Sensor Approaches



Hybrid Pixel Chip Assembly

Planar Sensor

- current design is an n-in-n planar sensor

3D Silicon

- Both electrode types are processed inside the detector bulk instead of

CVD (Diamond)

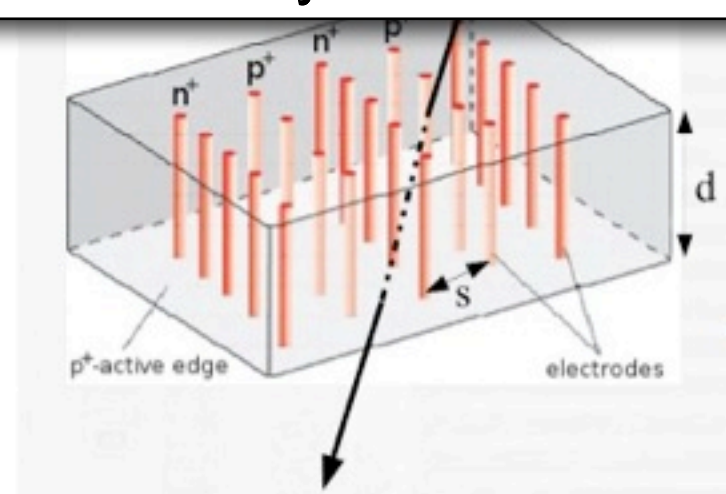
- Poly crystalline and single crystal

To bring to the lowest risk the IBL production – Be ready for a 100% planar solution, In case of low production yield of 3D sensor

Planar sensors (100%) are now ordered. Remaining 3D sensors contract is next (total 3+3 batches)!
Bump bonding of 100% planar and 25% 3D

Verify in February 2012 where we stand, before start loading on stave – Move then to a 100% planar scenario if necessary

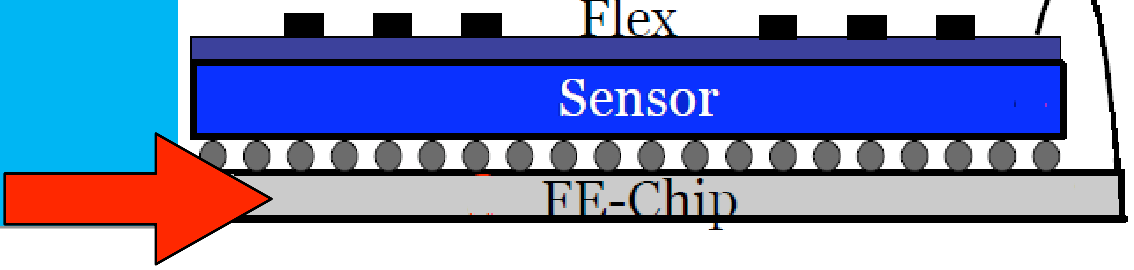
- problem. HV might need to exceed 1000V



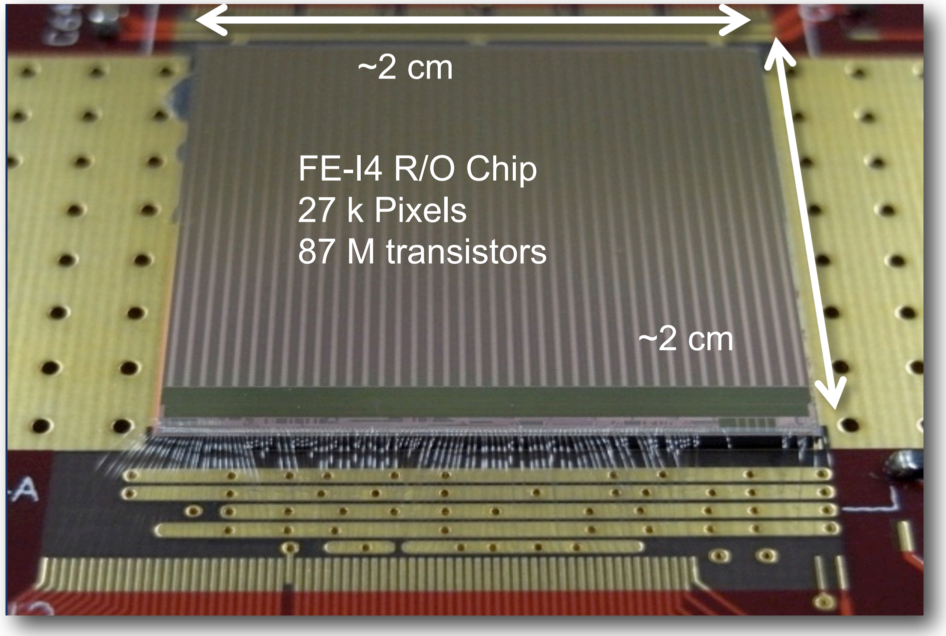
same X_0, but better S/N ratio (no dark current)

Review in July 2011 to decide which technology to be used for IBL

New FE-I4 Chip



- Reason for a new front-end chip
- Increased radiation hardness (> 250 MRad)
- New architecture to reduce inefficiencies (L=2x10^{34}): faster shaping; don't move hits from pixel until LVL1 trigger.
- Smaller pixel size 50 x 250 μm^2 (achieved by 0.13 μm CMOS with 8 metals)
- Larger fraction of footprint devoted to pixel array (~90%)
- Run 1 wafers received and used for various tests
- Tests
  - Very high yield (6 wafers fully tested, yield ~70%).
- Irradiated with protons
  - 6, 75 and 200 Mrad. All chips working after irradiation. Analog performance little affected (Noise, Threshold).
  - Analog performance is very good:
  - Low number of bugs and changes for final version, submission of final version planned soon (20-25 September, 44 days process time)



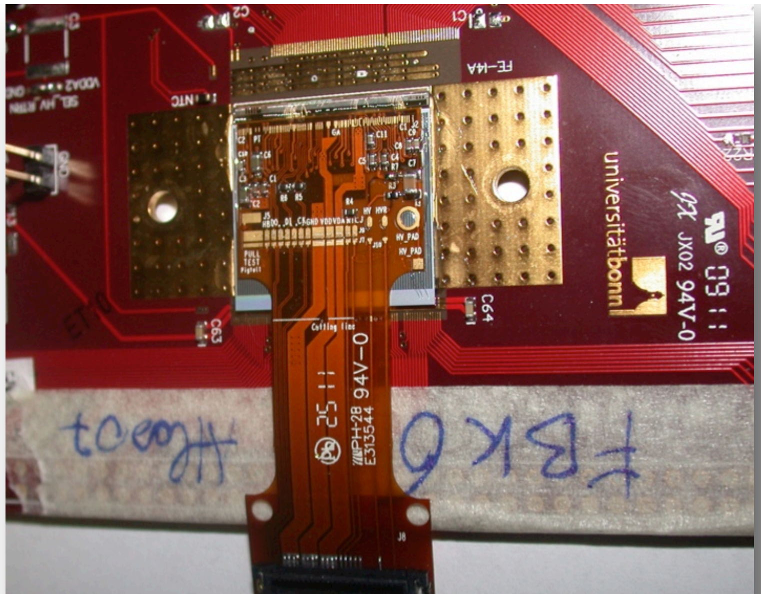
Modules & Staves

Modules:

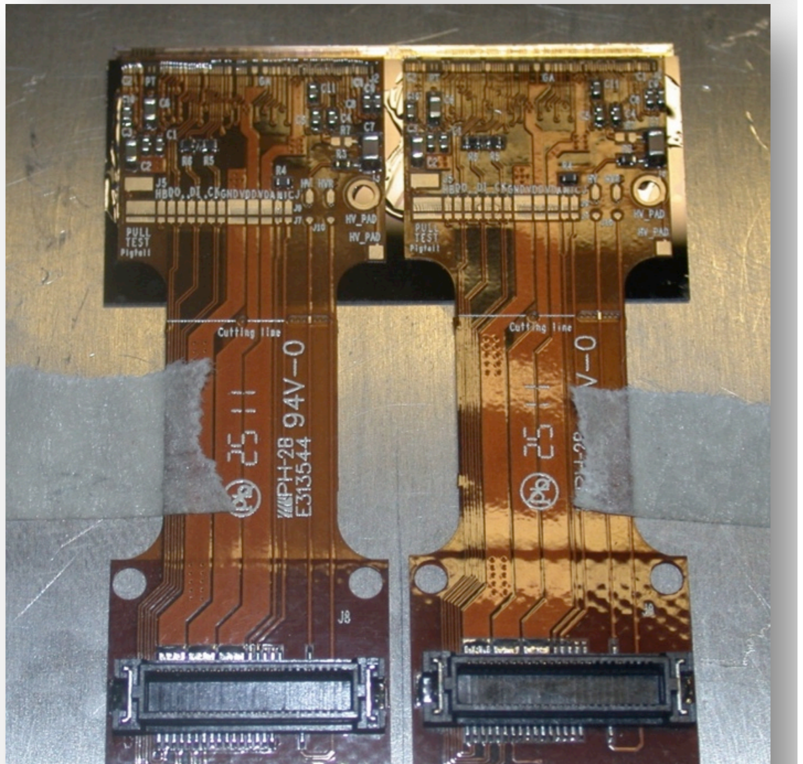
- First flex modules made and characterized.
- Digital flex modules (FE-I4 with glued silicon dummy sensors). Aim is gaining experience with stave loading by using mechanical component near to real. Wirebond to FE and real flex allow testing R/O and Power.

Stave prototypes:

- “Stave -1” : digital flex modules – test loading and system test – load during Sept/Oct; test with off-detector system Nov 2011-Jan 2012
- “Stave 0” : fully functional modules with thin FEI-4A: loading tests with full IBL modules: produce 40 planar and up to 20 3D modules in next 2-3 months – sufficient for 2 “stave-0” Double chip “digital module”



Real sensor single chip module


Double chip “digital module”

IBL Schedule

Activities	Starting	Ending
FEI4-B	Sept 11: Submission	Nov to Dec 11 for wafer tests
Bump bonding	Oct 11: pre-production	Aug/Sept: Completion
Module assembly	March 12:1st modules ready for loading	Dec 12 depending of sensor (2 mo contingency incl.)
Module loading	May 12: → 4 staves to be ready by June 12	Jan 13: Completion (2 mo contingency incl.)
Stave loading	Nov 12: starting with the 1st available staves	June/July 13: Completion
Final tests and commissioning	Sept 12 (beam pipe delivery to ATLAS)	Sept 13: IBL Installation (3 mo contingency incl.)

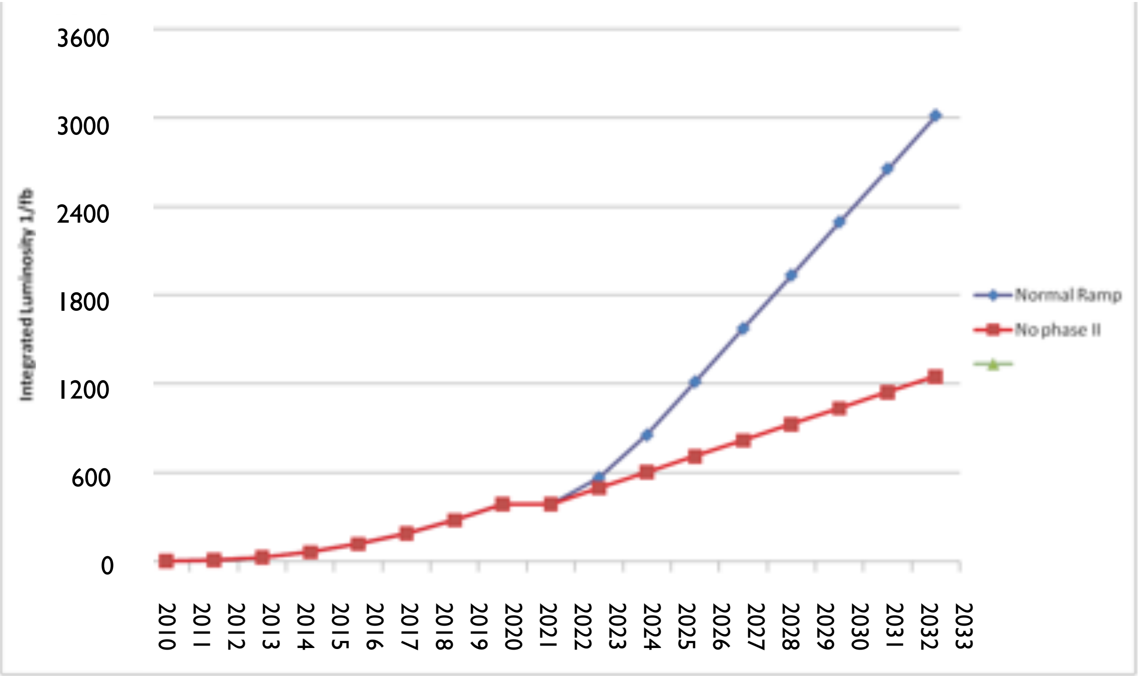
- Schedule is currently driven by FEI4 Version B delivery
- Technically they are prepared for 100% production of planar modules and 25% production of 3D modules
- Prioritize planar modules for first modules to “learn” FEI4 Version B chip and module assembly
- Production schedule at IZM with increased number of modules compatible with IBL schedule (higher throughput than planned)
- Work at IZM extended by ~ 2 months for additional modules (125%), but overall faster through put gains -> in schedule
- First modules are expected by March 2012!

Phase 2 Upgrade (2022 Shutdown LS3)

Upgrading the ATLAS Experiment

To keep ATLAS and CMS running beyond ~10 years requires tracker replacement
Current trackers designed to survive up to 10MRad in strip detectors (≤ 700 fb^{-1})
For the luminosity-upgrade the new trackers will have to cope with:

- much higher integrated doses (need to plan for 3000 fb^{-1})
- much higher occupancy levels (up to 200 collisions per beam crossing)
- Installation inside an existing 4π coverage experiment



- Budgets are likely to be such that replacement trackers, while needing higher performance to cope with the extreme environment, cannot cost more than the ones they replace

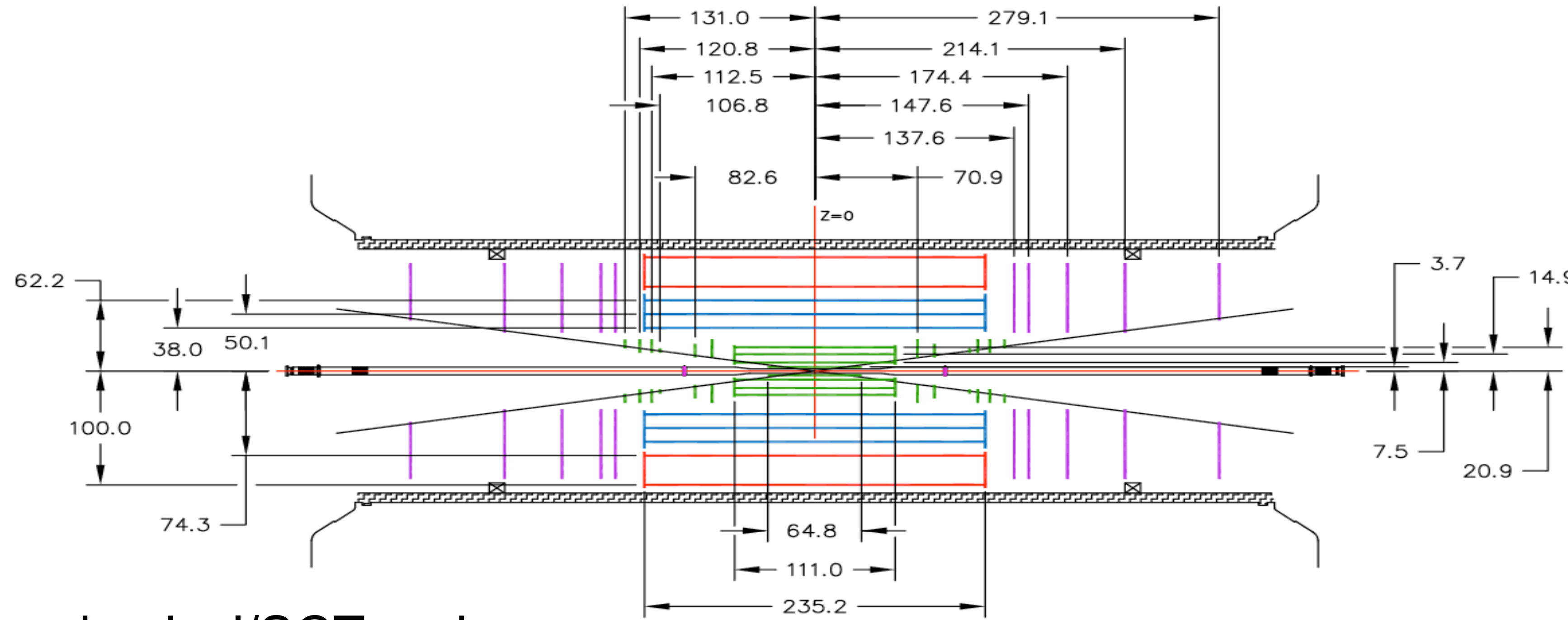
To complete a new tracker by ~2020, require Technical Design Report 2014/15
(Note the ATLAS Tracker TDR: April 1997; CMS Tracker TDR: April 1998)

Possible Technologies (Active Element)

Section	Radius (cm)	Area (m^2) (*1)	Fluence (neq/cm^{-2}) (*2)	Technologies/Vendor capability
B-Layer	3.7	~0.2	~2.2×10^{16}	Diamond, 3D, Planar, GOSSIP, Exotic, … (highly radiation-tolerant)
Inner Pixel	7.5	~0.8	~6×10^{15}	3D, Planar, … (medium area - low cost)
Outer Pixels	15.5 – 19.5	~5.6	~2×10^{15}	Planar (large area – low cost) Large-scale production capability
Strips	30 e.g.	~200	~1×10^{15}	Strips (large area – low cost) Large-scale production capability

Notes:
(*1) Utopia H, and including +30% contingency
(*2) Fluences assumption with 3000 fb-1 and with safety factor 2

UTOPIA Layout

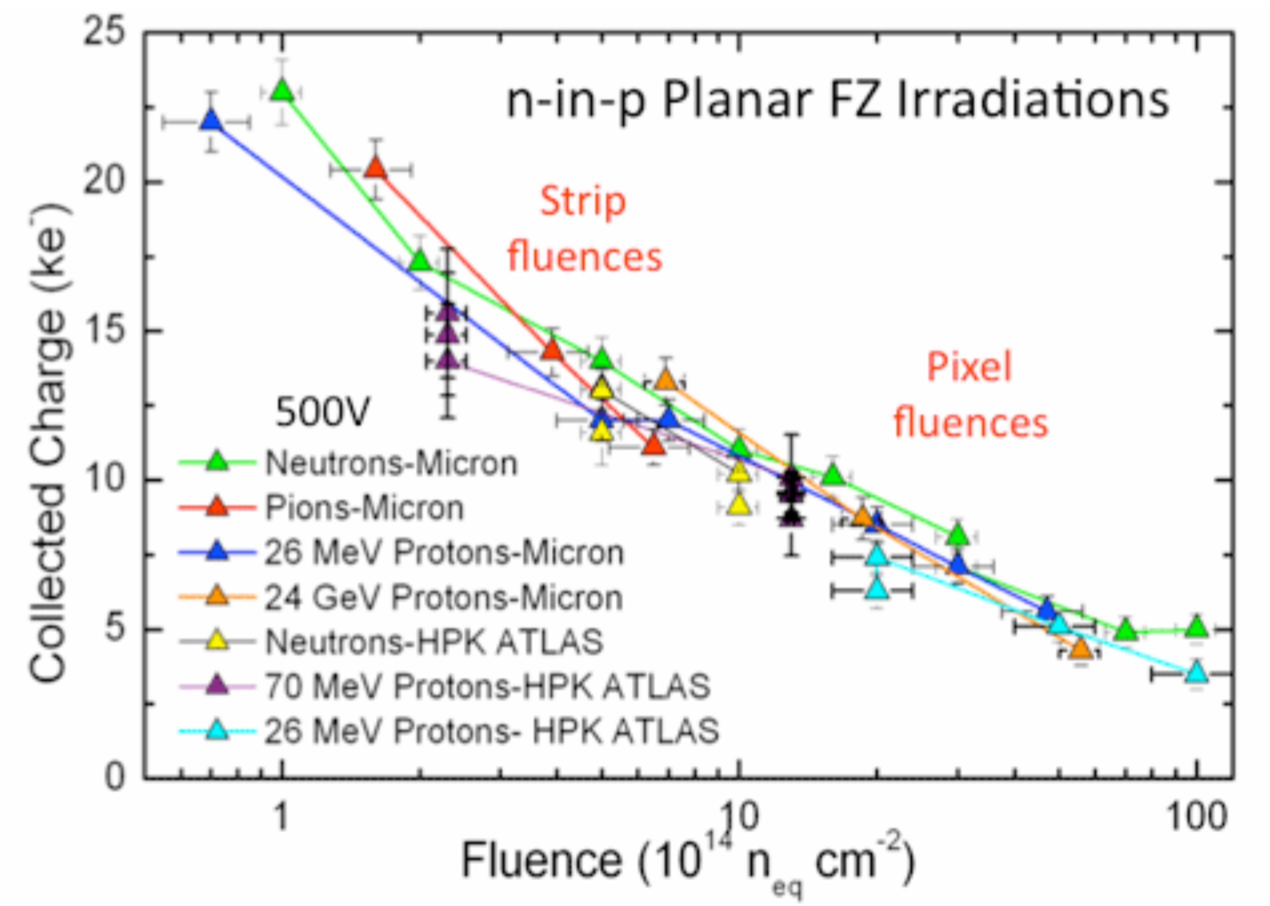


- Current ATLAS!
- Same number of silicon layers in pixel/SCT region
- TRT replaced by two layers of long-strip silicon: This has the same effective resolution as the TRT (but not the pattern recognition ability and no PID)
- SCT --> Short strips
  - One less layer (turned to pixels)
- Pixels region
  - Increase number of layers for better track seeding and fake rejection
  - Reduce pixel size to increase granularity
  - Granularity guided by "keep occupancy < 1 %" Not achieved everywhere!
- Si-to-Si total length <= 6 m for insertion in ATLAS in one piece

I will concentrate on the Silicon Strip Detector R&D

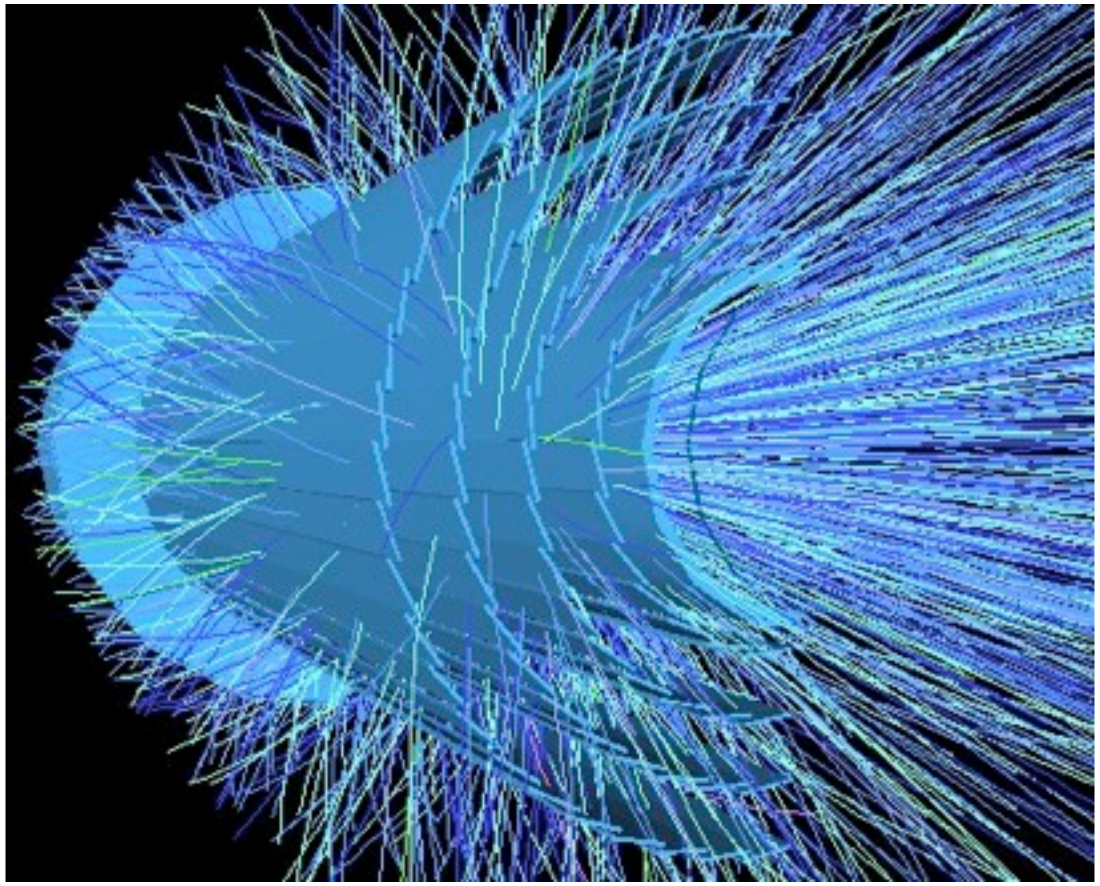
Main Concerns for the Detectors

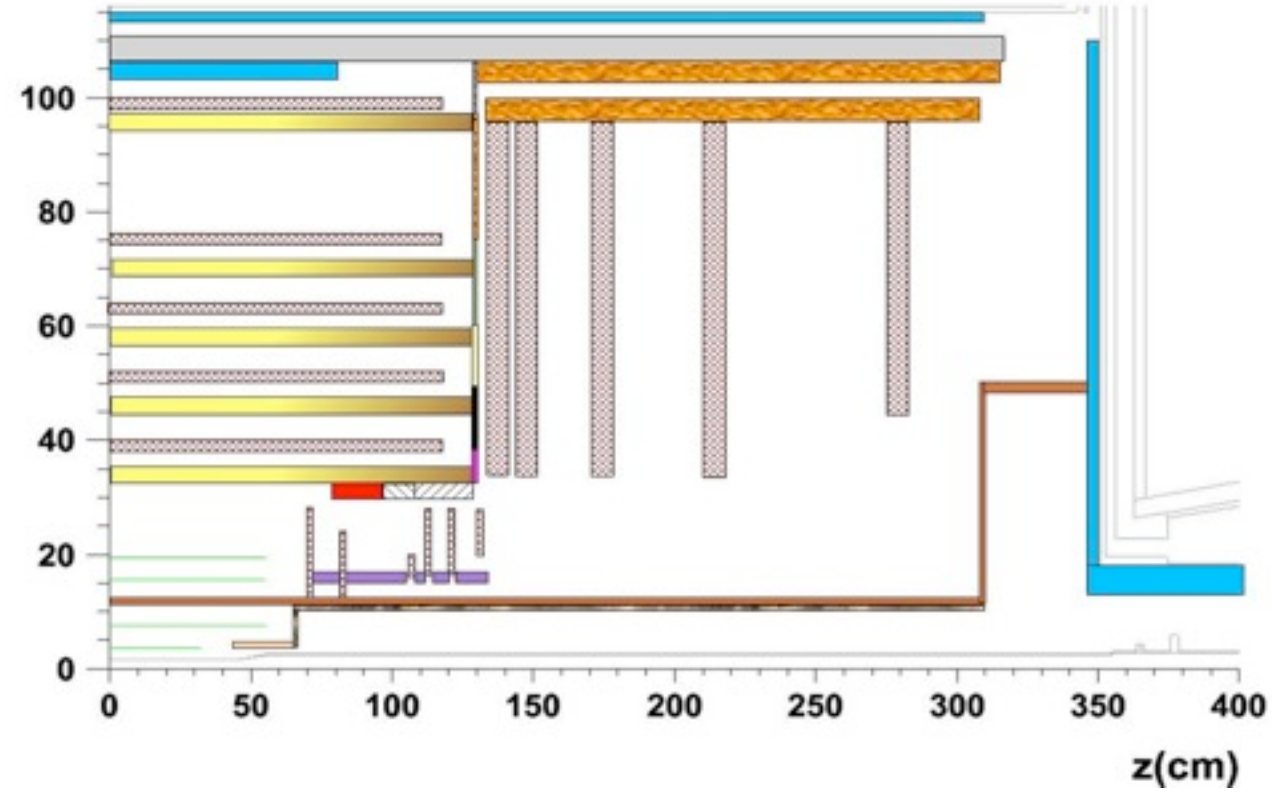
- Detector aging (Si detectors, Scintillators, LAr electronics, FCAL, ….)
- High level of pile-up : design for max mu=200
- New radiation environment (up to 10^{17} n/cm^2)
- High occupancy (TRT out, more difficult trigger and tracking conditions)



- Technology aging in many parts of the detector and infrastructure (electronics, controls, safety systems, …)
- Radiation contamination (difficult access, waste material, …)
- Possible new optics conditions from the LHC (aperture limitations, ….)
- …

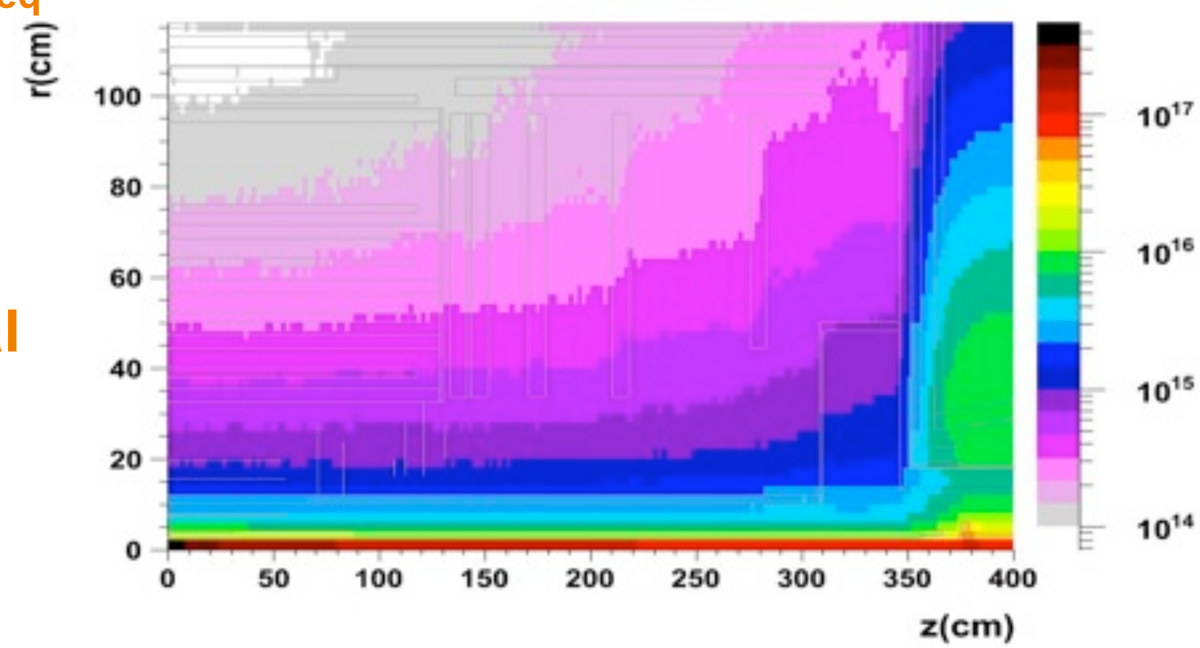
Radiation Background Simulation





1 MeV neutron eq fluence

At inner pixel radii - target survival to 2×10^{16} n_{eq}/cm^2



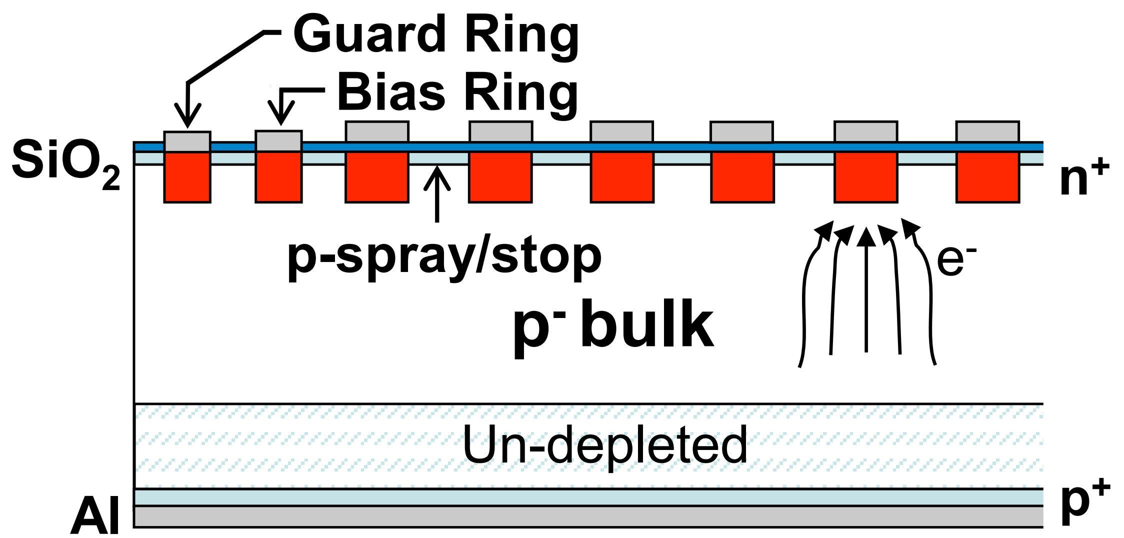
Numbers obtained 9/10/09 (corresponding to new layout) assuming 3000fb-1 and 84.5mb

Strip barrel 1 (SS)	(r=38cm; z=0cm)	4.4x10^14
	(r=38cm; z=117cm)	4.9x10^14
Strip barrel 4 (LS)	(r=74.3cm; z=0.0cm)	1.6x10^14
	(r=74.3cm; z=117cm)	1.8x10^14
Strip Disc 1 (z=137.1, Rinner=33.6)		6.0x10^14
Strip Disc 2 (z=147.6, Rinner=33.6)		6.2x10^14
Strip Disc 3 (z=174.4, Rinner=33.6)		5.8x10^14
Strip Disc 4 (z=214.1, Rinner=33.6)		6.1x10^14
Strip Disc 5 (z=279.1, Rinner=44.4)		5.8x10^14
Strip Disc 5 (z=279.1, Rinner=54.1)		4.4x10^14
Strip Disc 5 (z=279.1, Rinner=61.7)		3.9x10^14
new		
Strip Disc 5 (z=279.1, Rinner=73.6)		3.0x10^14
Strip Disc 5 (z=279.1, Rinner=84.9)		2.7x10^14

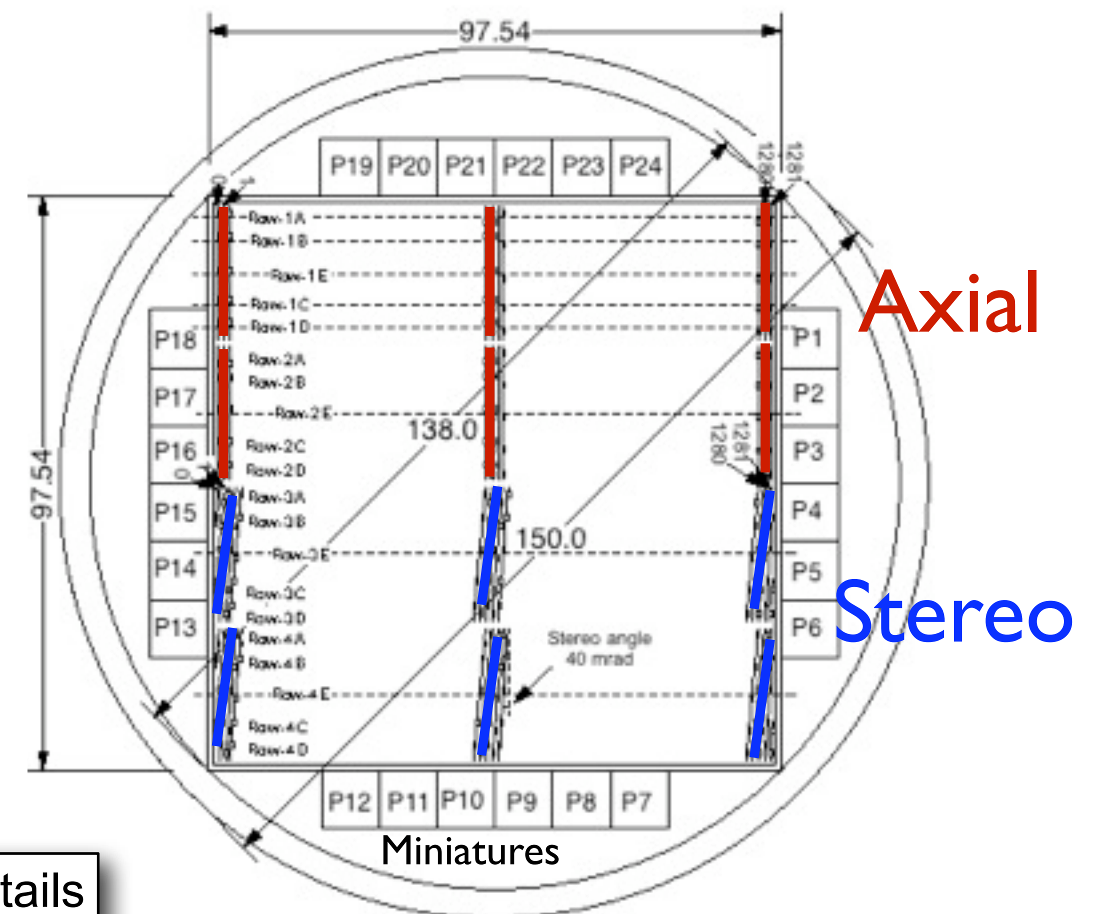
For strips $3000fb^{-1}$ ×2 implies survival required up to ~2×10^{15} n_{eq}/cm^2

Radiation Hard Sensors

- n⁺-strip in p-type substrate (n-in-p)
  - Collects electrons like current n-in-n pixels
    - Faster signal, reduced charge trapping
  - Always depletes from the segmented side
    - Good signal even under-depleted
  - Single-sided process
    - ~50% cheaper than n-in-n
    - More foundries and available capacity world-wide
  - Easier handling/testing due to lack of patterned back-side implant

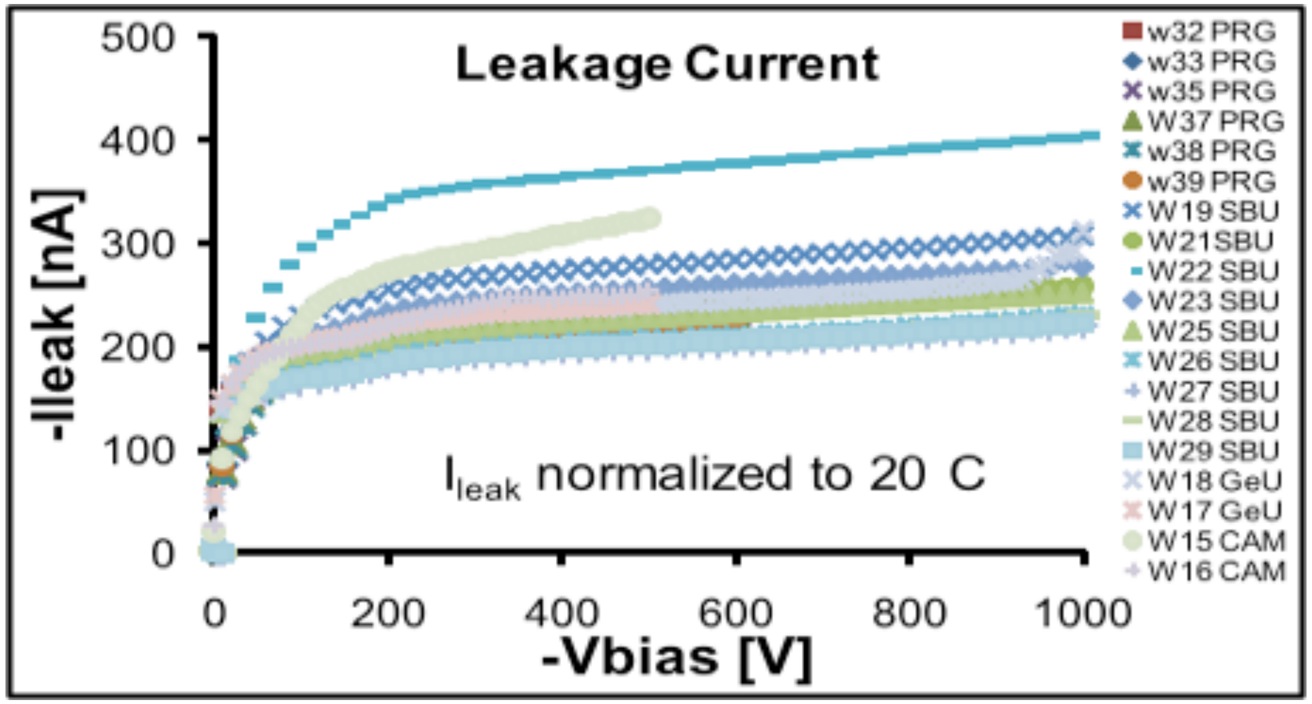


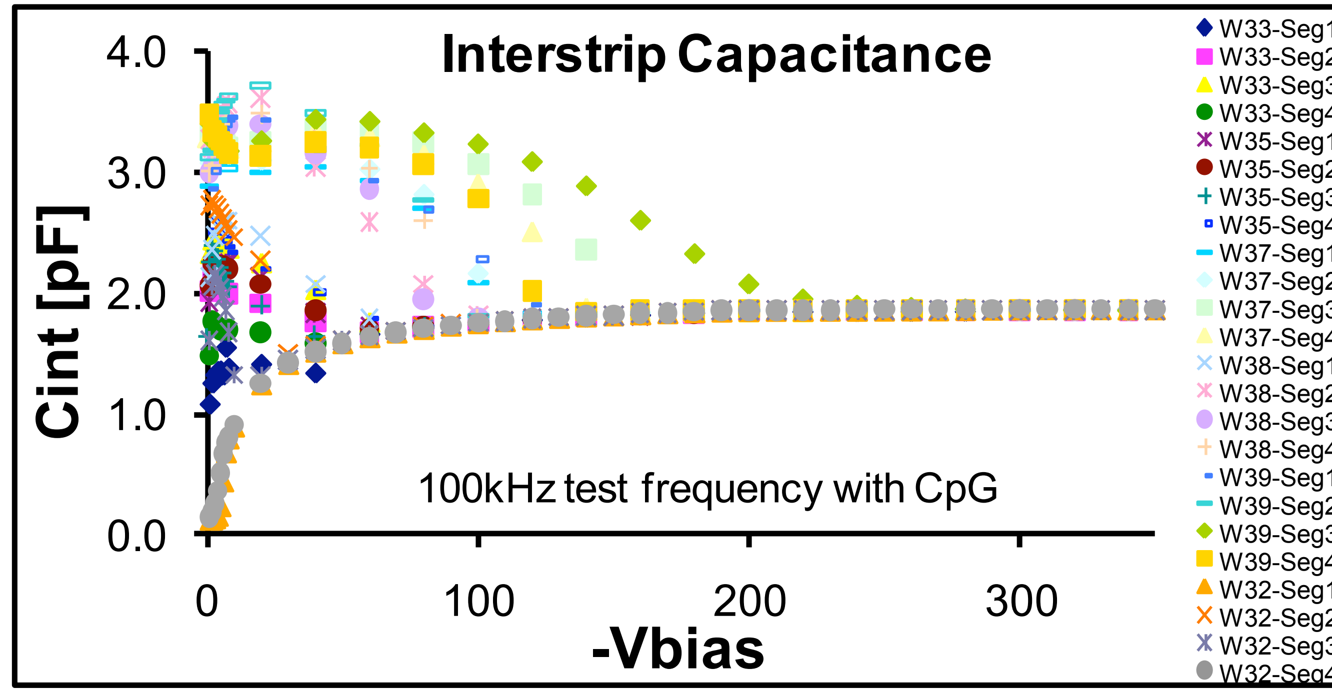
- Collaboration of ATLAS with Hamamatsu Photonics (HPK) to develop 9.75x9.75 cm² devices (6 inch wafers)
  - 4 segments (2 axial, 2 stereo), 1280 strip each, 74.5 µm pitch, ~320 µm thick
  - FZ1 <100> and FZ2 <100> material studied
  - Miniature sensors (1x1 cm²) for irradiation studies

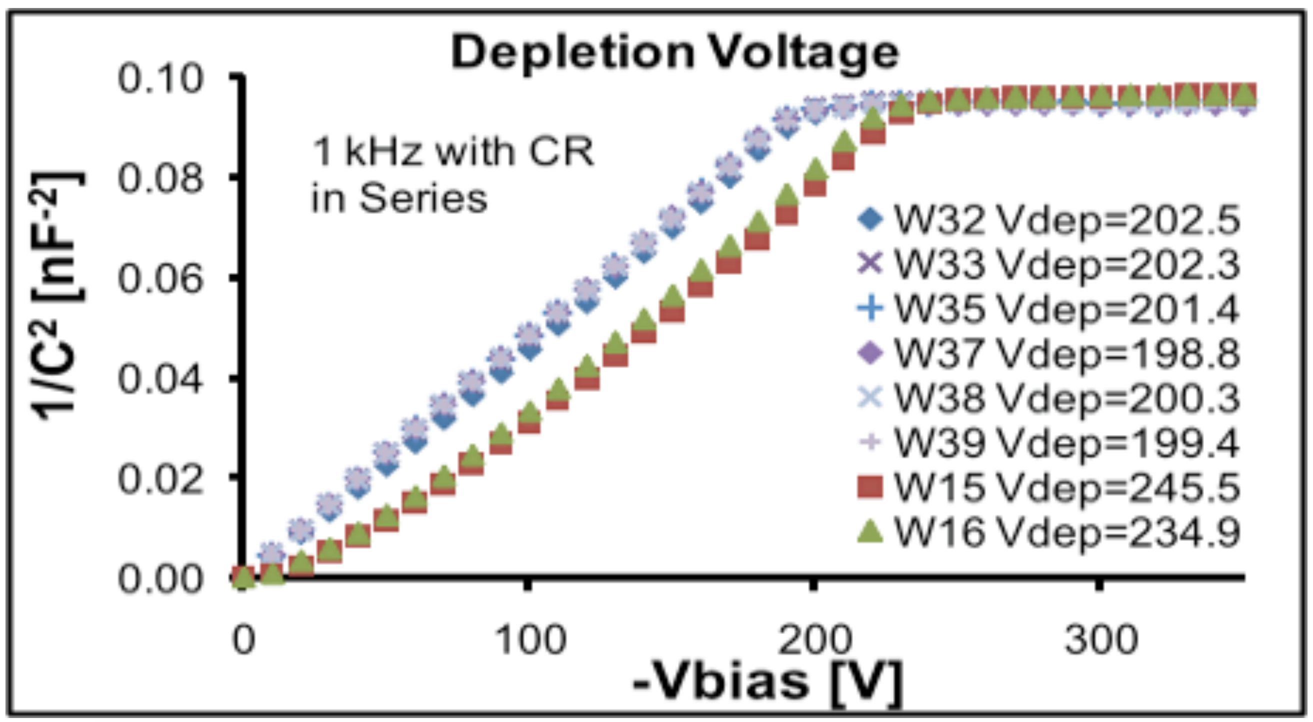


See N. Unno, et. al., Nucl. Inst. Meth. A, Vol. 636 (2011) S24-S30 for details

Full-size Sensor Evaluation





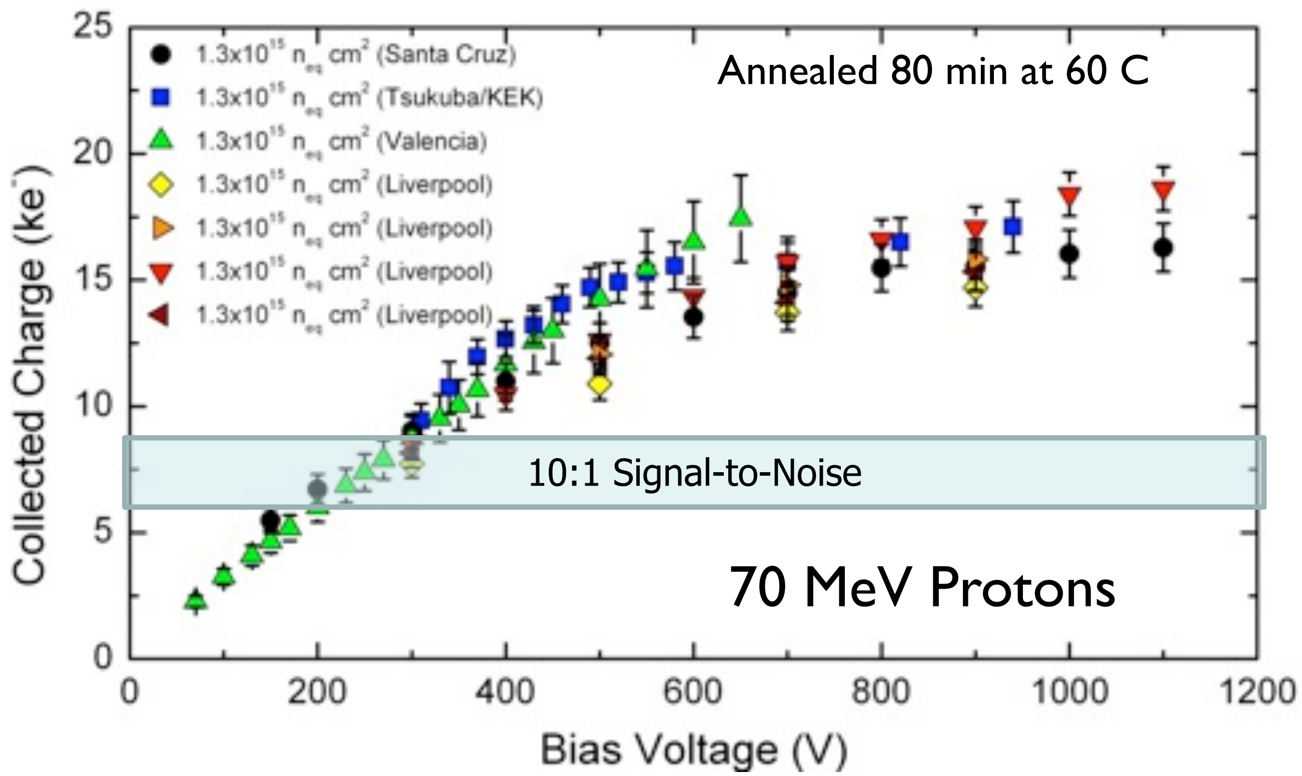


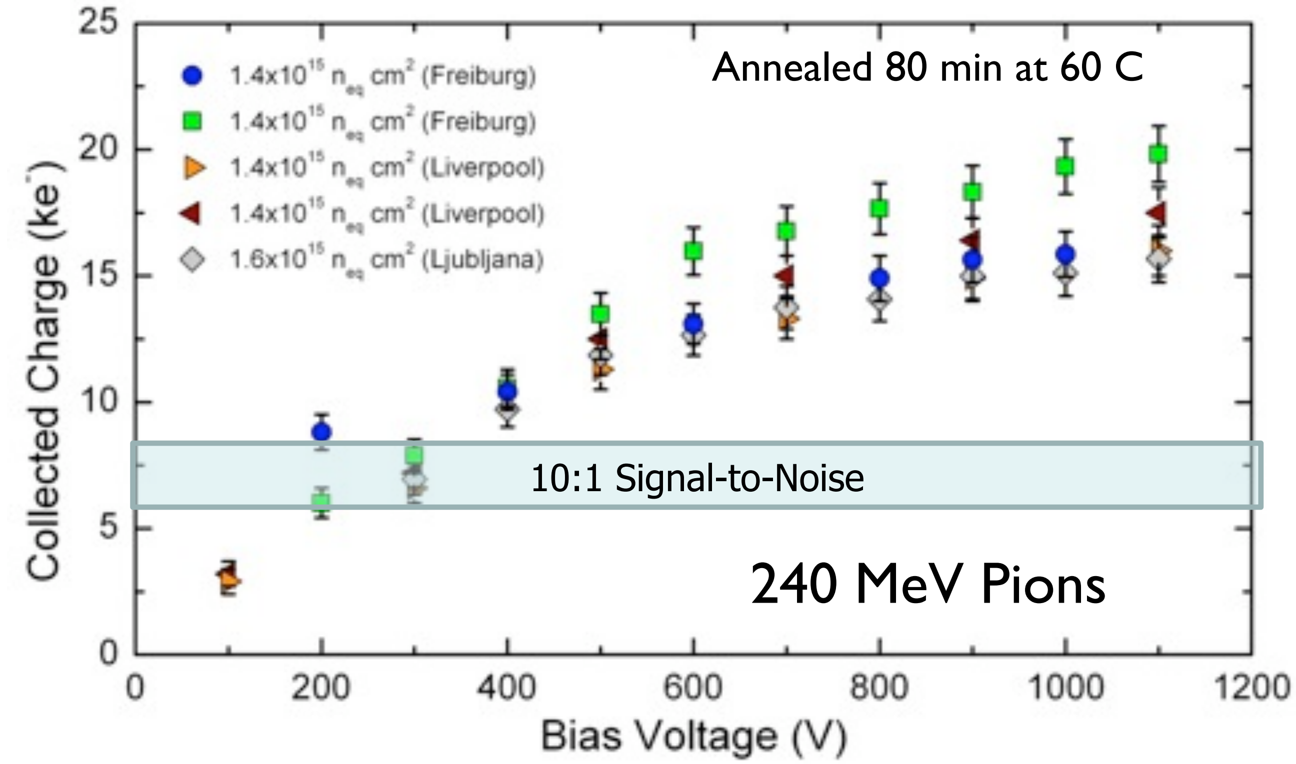
See J. Bohm, et. al., Nucl. Inst. Meth. A, Vol. 636 (2011) S104-S110 for details

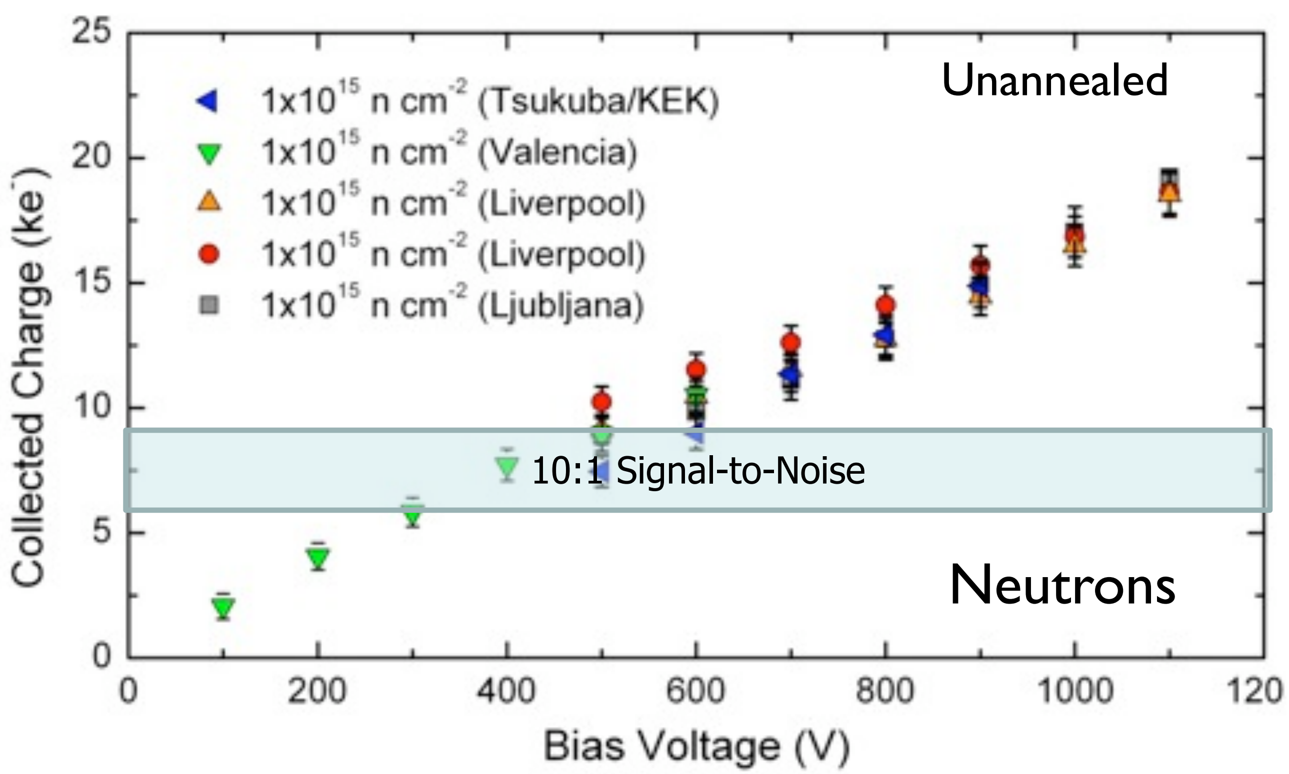
	Specification	Measurement
Leakage Current	<200 μA at 600 V	200– 370nA
Full Depletion Voltage	<500 V	190 – 245V
Coupling Capacitance (1kHz)	>20 pF/cm	24 – 30pF
Polysilicon Resistance	1.5+/-0.5MΩ	1.3 -1.6MΩ
Current through dielectric	I_{diel} < 10 nA	< 5nA
Strip Current	No explicit limit	< 2nA
Interstrip Capacitance (100kHz)	<1.1pF/cm (3 probe)	0.7 – 0.8pF
Interstrip Resistance	> 10x R_{bias}~15 MΩ	>19 GΩ

All specifications already met!!

Charge Collection Results



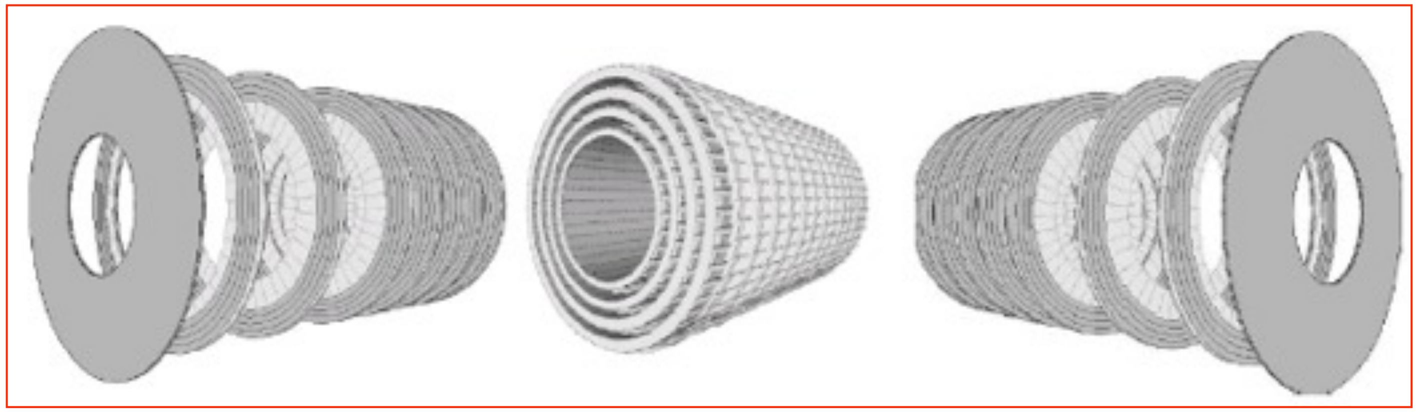




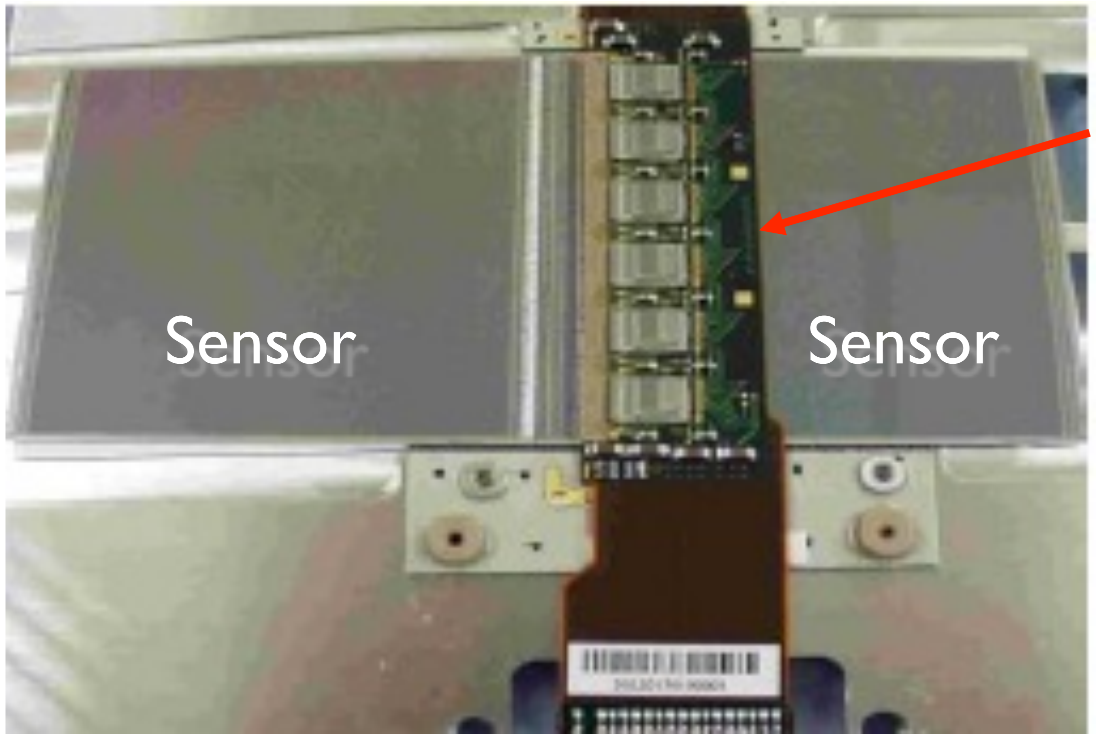
- Miniature devices irradiated to strip barrel fluences with neutrons, pions, protons
- Charge collection measured with ^{90}Sr β-source
  - Consistent results between different groups/equipment
- S/N greater than 10:1 for strip sensor types with expected noise performance
  - ~600-800 e$^-$ short strips, ~800-1000 e$^-$ long strips
  - See H. Sadrozinski, et.al., Nucl. Inst. Meth. A, doi: 10.1016/j.nima.2011.04.0646 for details

Current SCT ATLAS Module Designs

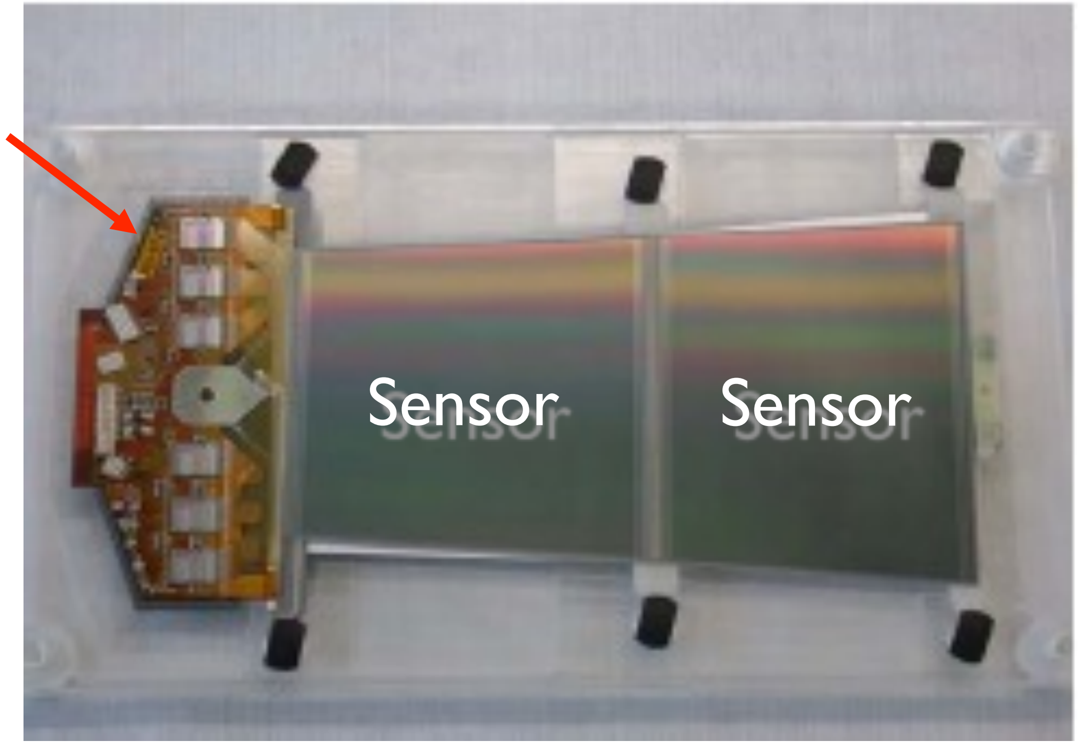
ATLAS Tracker Based on
Barrel and Disc Supports



Effectively two styles of double-sided modules (2×6cm long)
each sensor ~6cm wide (768 strips of 80μm pitch per side)



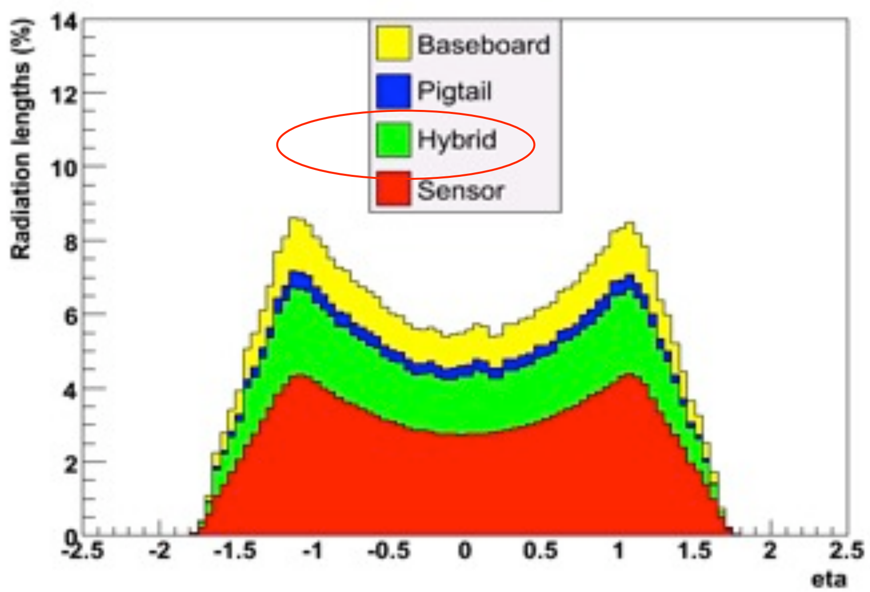
Hybrid cards carrying read- out chips and multilayer interconnect circuit



Barrel Modules
(Hybrid bridge above sensors)

Forward Modules
(Hybrid at module end)

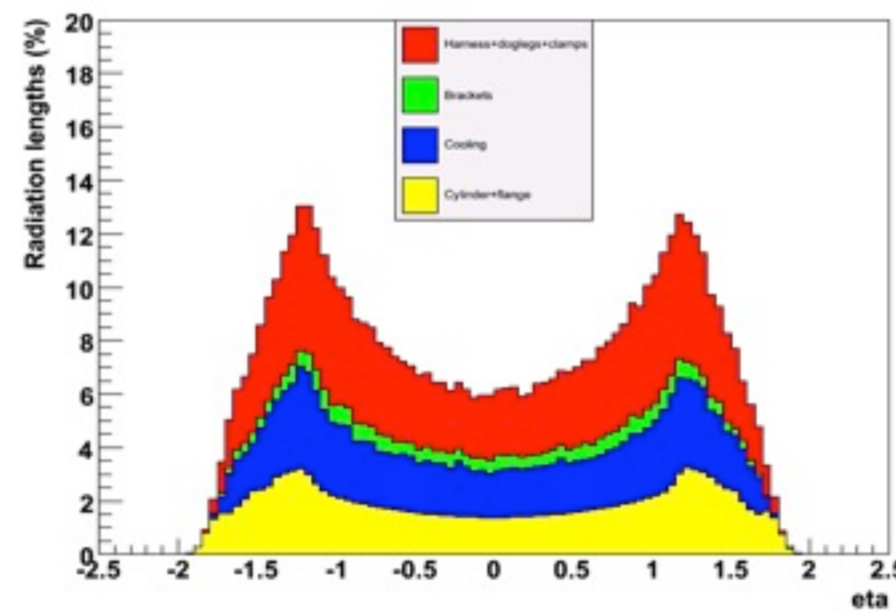
Current Silicon Microstrip (SCT) Material



Old ATLAS Barrel Module

12 ASIC of 300μm thickness for double-sided module read-out

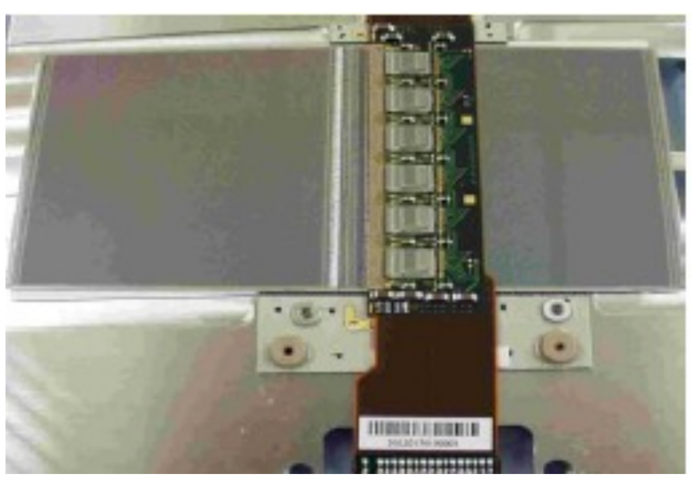
(*ie* just 6 read-out chips per side)



“The barrel modules of the ATLAS semiconductor tracker”. Nucl.Instrum.Meth.A568:642-671,2006.

Table 1
Radiation lengths and weights estimated for the SCT barrel module

Component	Radiation length [%Xo]	Weight [gr]	Fraction [%]
Silicon sensors and adhesives	0.612	10.9	44
Baseboard and BeO facings	0.194	6.7	27
ASIC's and adhesives	0.063	1.0	4
Cu/Polyimide/CC hybrid	0.221	4.7	19
Surface mount components	0.076	1.6	6
Total	1.17	24.9	100

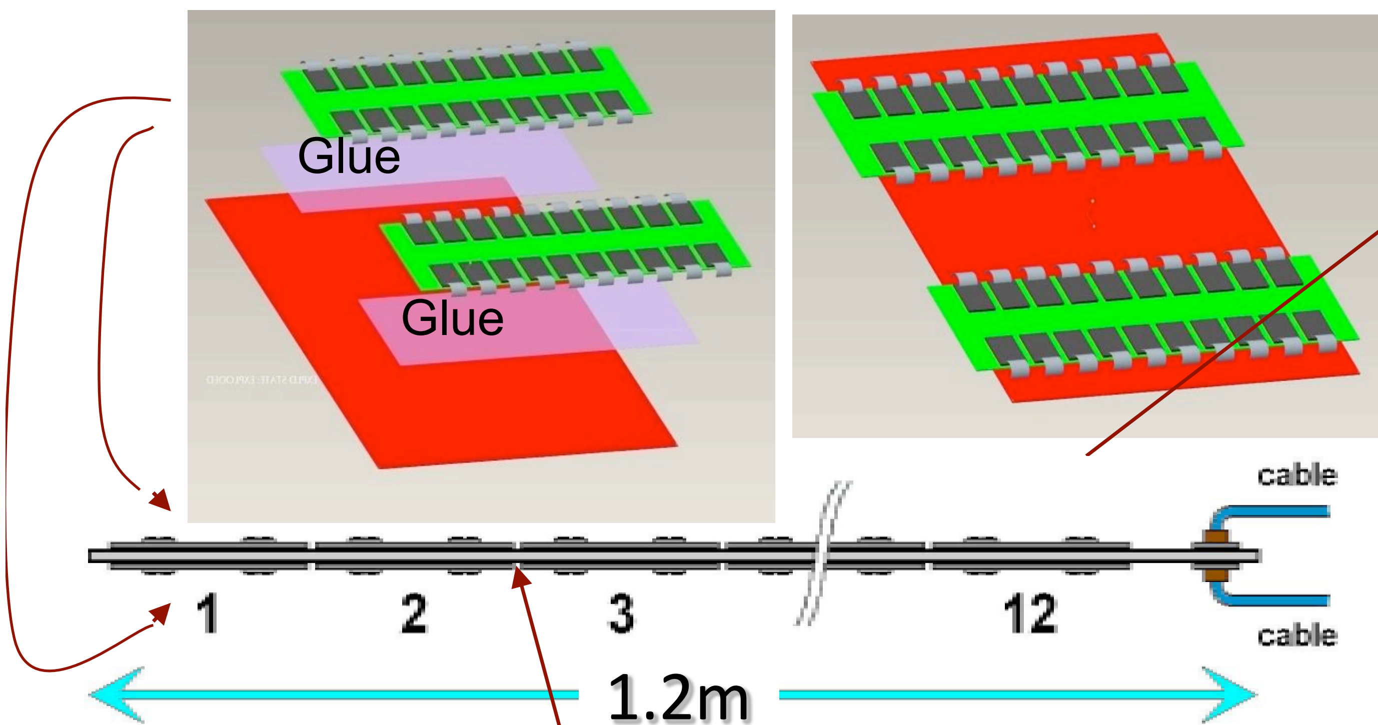


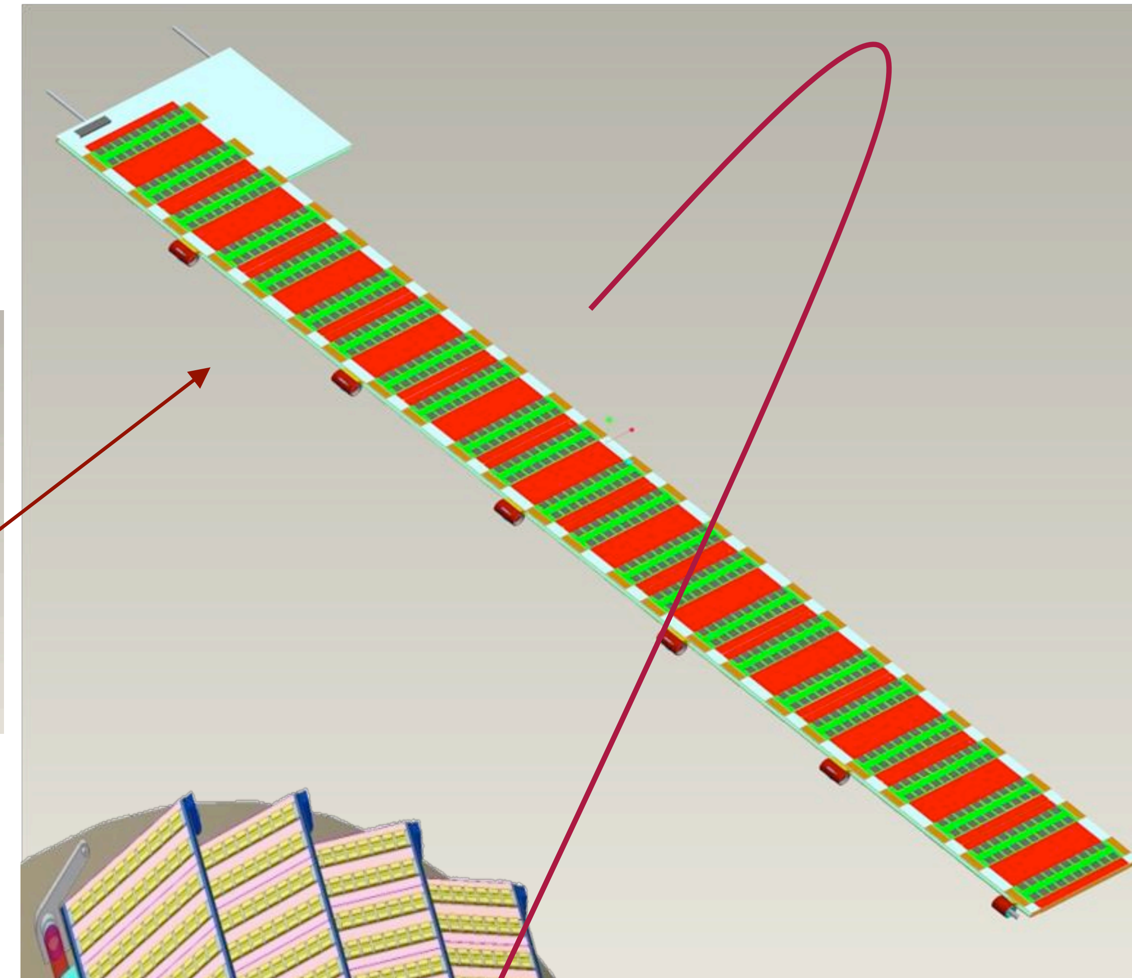
New ATLAS sLHC-Tracker Module will have 80 ASICs in two hybrid fingers for just one-sided read-out

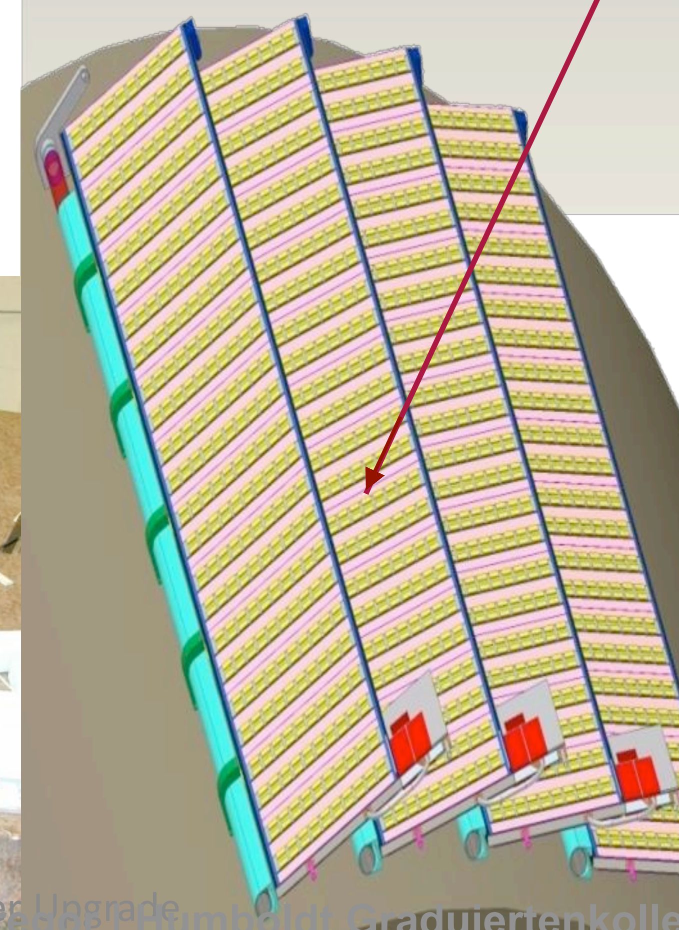
Hybrid area per module roughly ×2 at HL-LHC - much higher R/O granularity

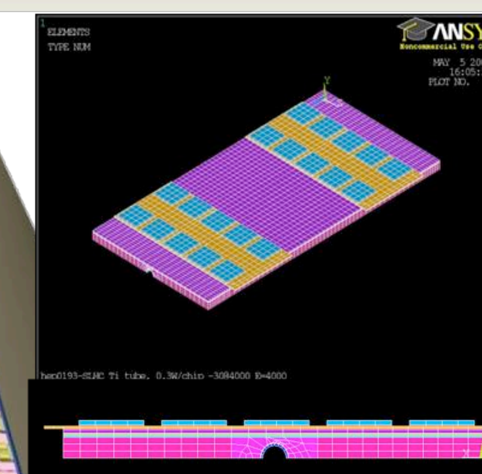
New Design (Phase 2)

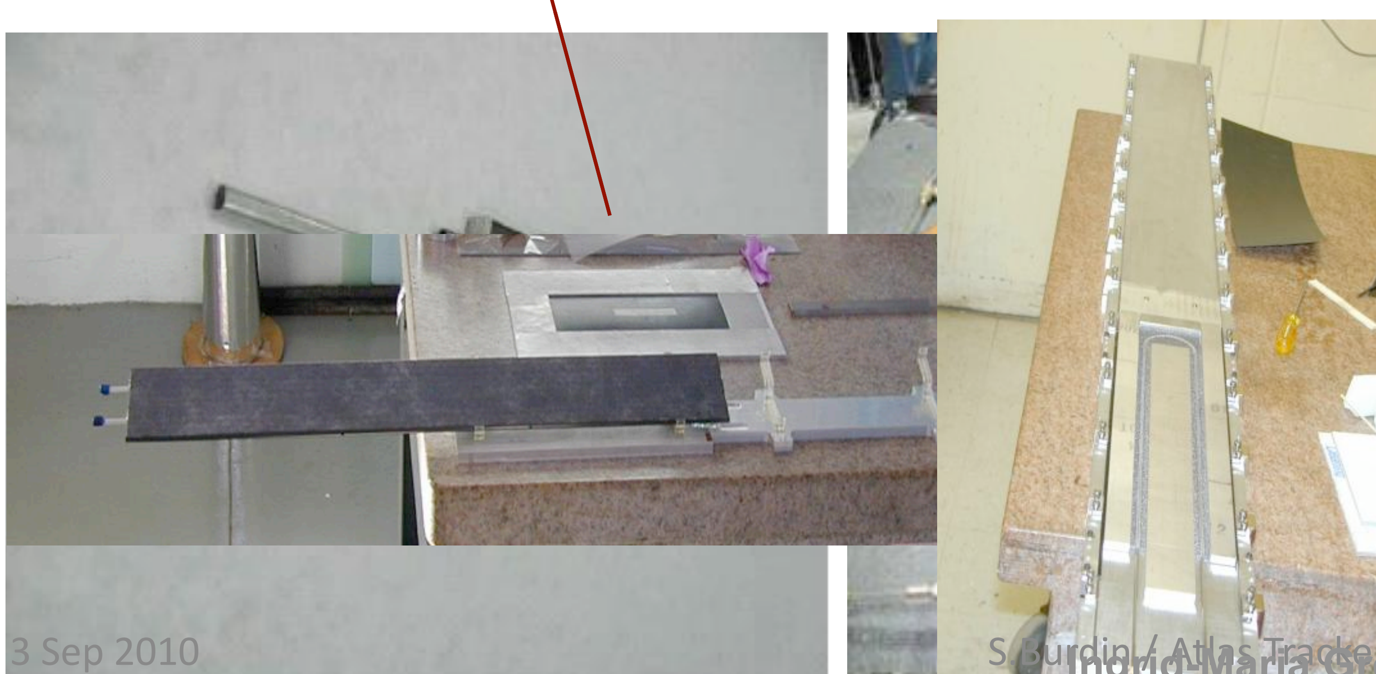
- Hybrid glued to sensors glued to bus tape glued to cooling









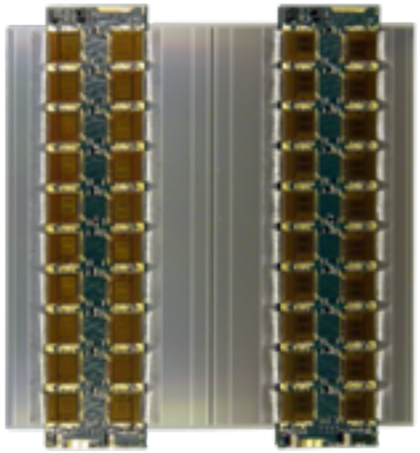


Stave+Petal Programme

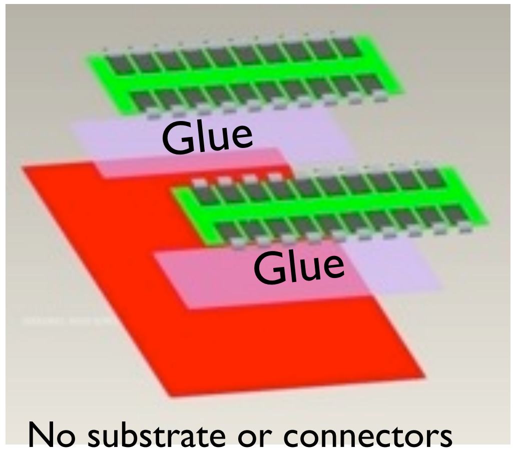
- Designed to reduce radiation length
  - Minimize material by shortening cooling path
  - Glue module directly to a stave core with embedded pipes

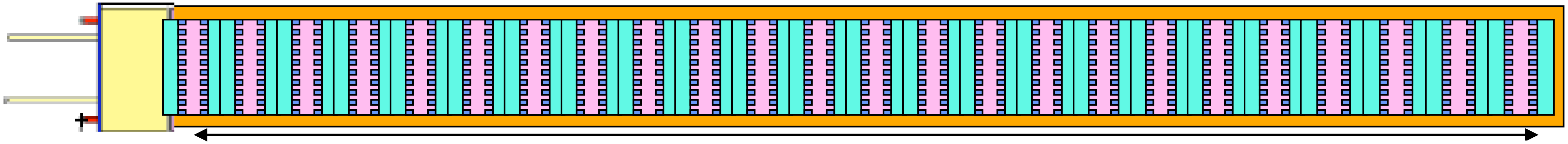
Petal Hybrid

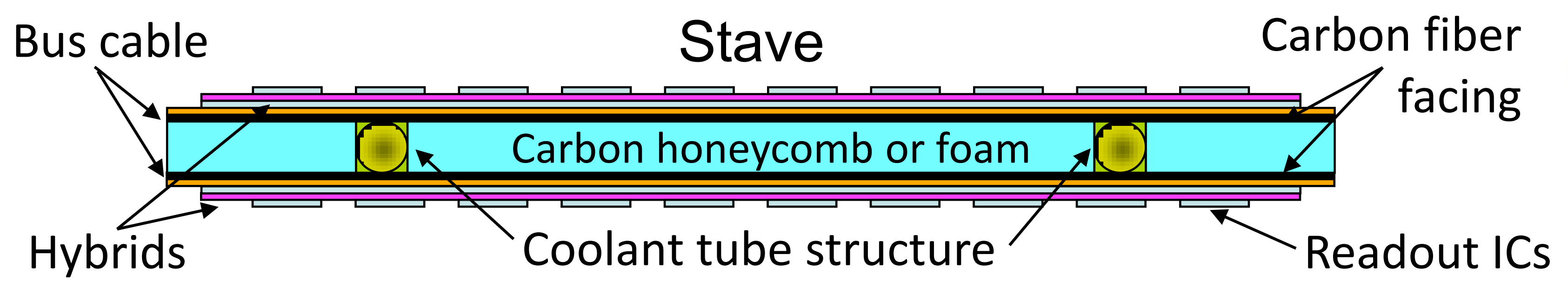
- Requirements of large scale assembly considered from the beginning-
  - Simplify build as much as possible
- All components independently testable prior construction
- Design aims to be low cost
- Minimize specialist components



Stave Module







Ongoing Work

Seven sites making progress with hybrid and module assembly/bonding/testing

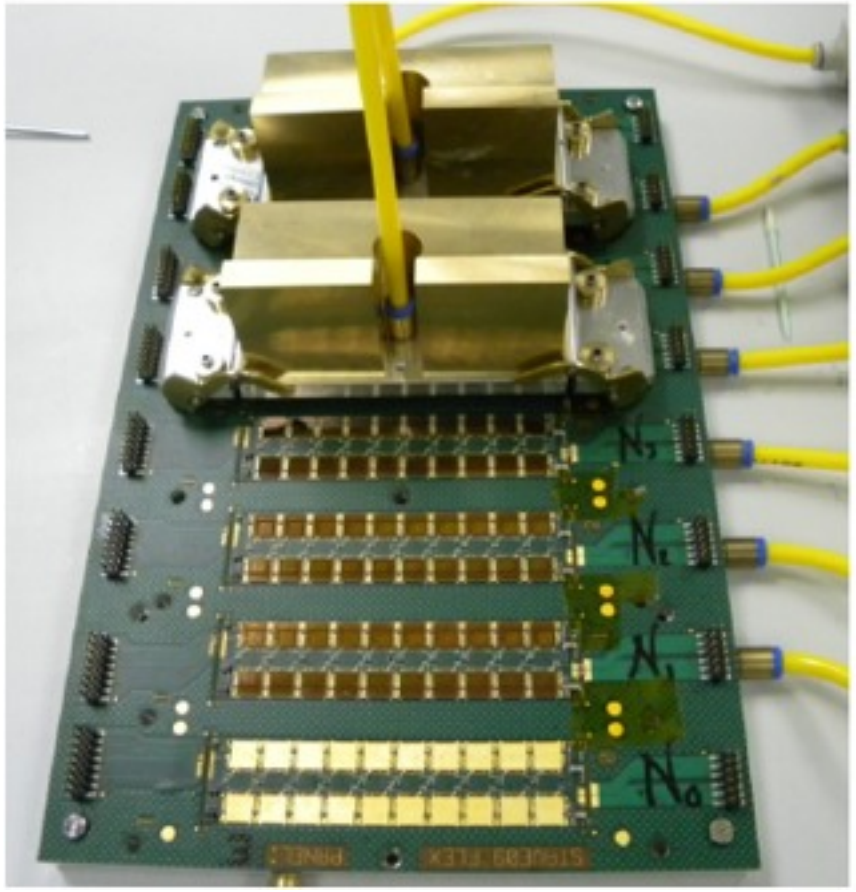
	← Hybrids →					← Modules →				
	Mechanical Chip Gluings	Mechanical Wirebonding	Electrical Chip Gluings	Electrical Wirebondings	Electrical Testing	Mechanical Assemblies	Mechanical Wire Bondings	Electrical Assemblies	Electrical Wire Bonding	Electrical Testing
Cambridge	✓	✓	✓	✓	✓	✓	✓ (yellow)	✓ (yellow)		
DESY	✓	✓ (yellow)	✓		✓	✓	✓ (yellow)	✓ (yellow)		
Freiburg	✓	✓B ✓EC	✓	✓ EC ✓B	✓	✓	✓	✓	✓	✓
Glasgow	✓ (yellow)									✓ (yellow)
LBL					✓	✓	✓	✓	✓	✓
Liverpool	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Santa Cruz	✓	✓	✓	✓	✓	✓	✓ (yellow)	✓ (yellow)	✓ (yellow)	

✓ indicates proficiency ✓ (yellow) indicates in process of becoming proficient

Plan on 1-2 months for sites to make electrical modules

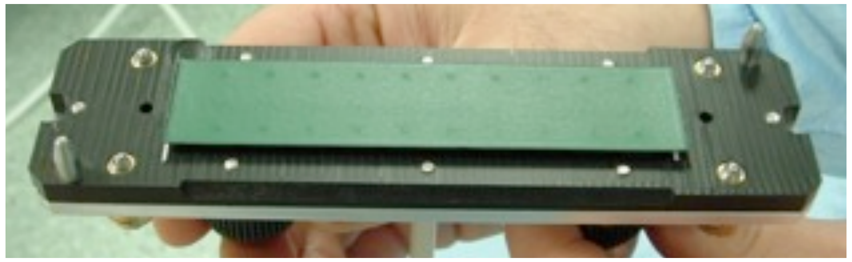
Hybrid Mass Production

- First pass at industrialization of hybrids:
  - Panelization (8 per panel):
    - Flex selectively laminated to FR4
      - FR4 acts as temporary substrate during assembly, wire bonding and testing
  - Designed for machine placement and solder re-flow of passive components
  - Mass attachment/wire bonding of custom ASICs
- Flex uses conservative design rules (~20000 hybrids to be installed):
  - ↳ High yield, large volume, low price
    - ➢ 100µm track and gap, blind vias (375µm lands within 150µm drill) and 50µm dielectrics
- Hybrids+ASICs tested in panel
  - With final ASIC set (ABCn-130nm, HCC, power), all hybrids in the panel tested with one data I/O and one power connection

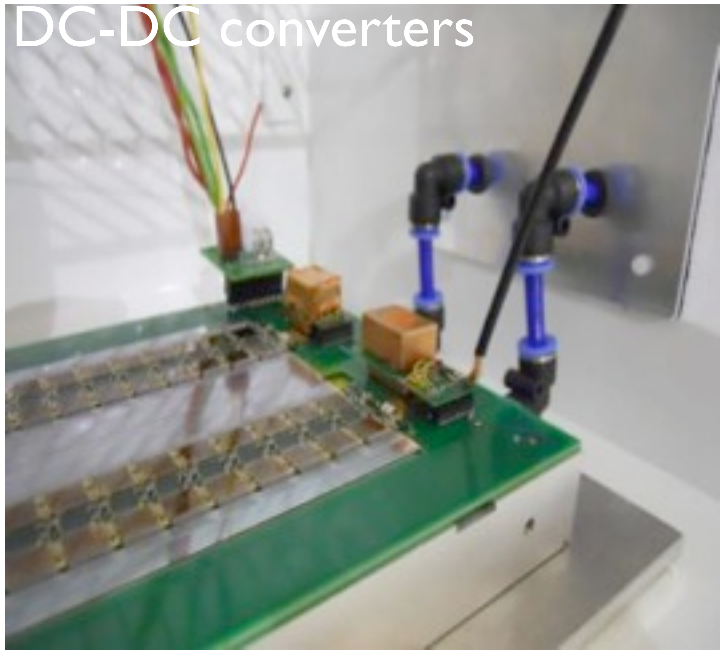


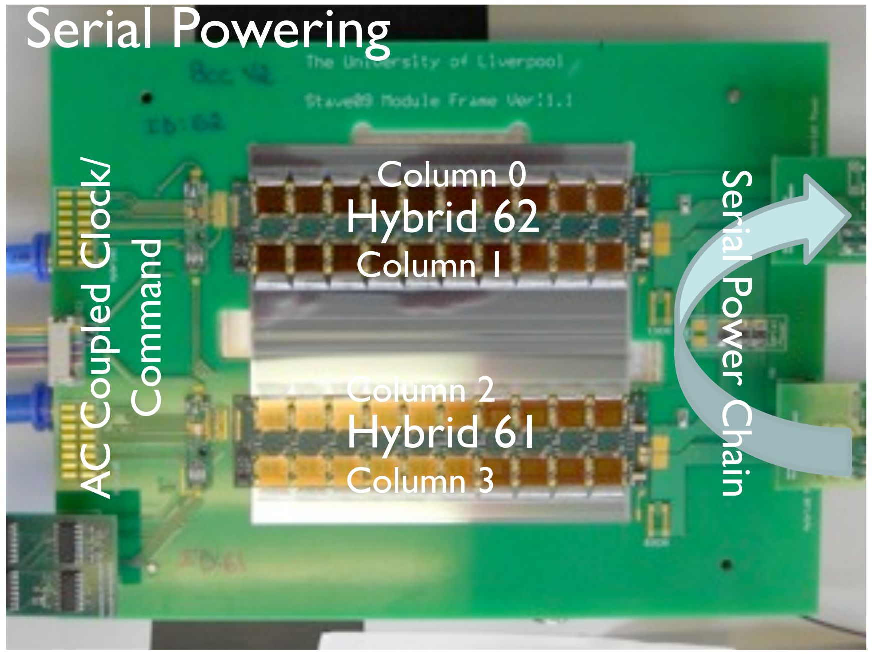
Panel dimensions: 300mm x 200mm
Hybrid dimensions: 24mm x 107.6mm

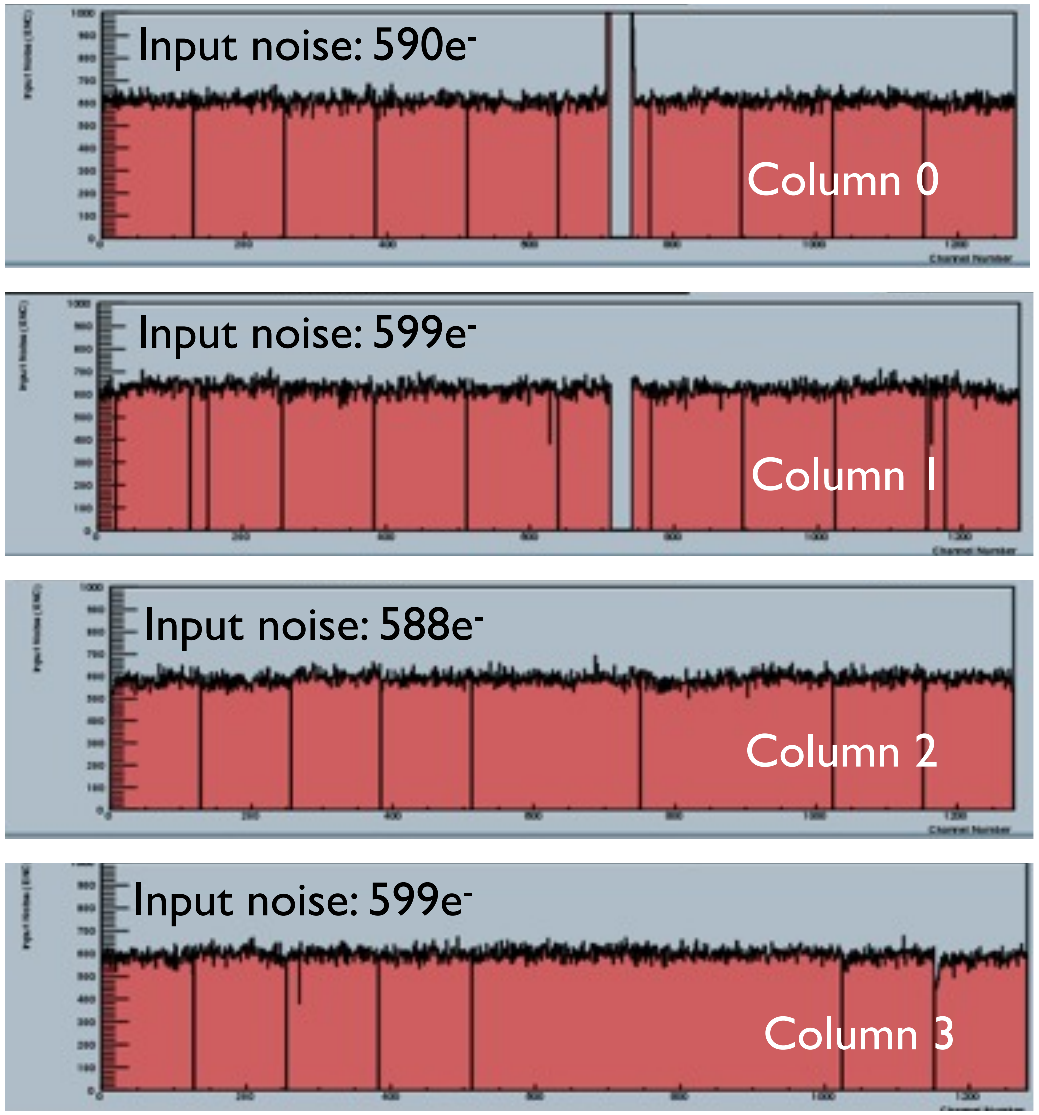
Fully characterized hybrid cut out of panel ready for module assembly



Stave Module Tests



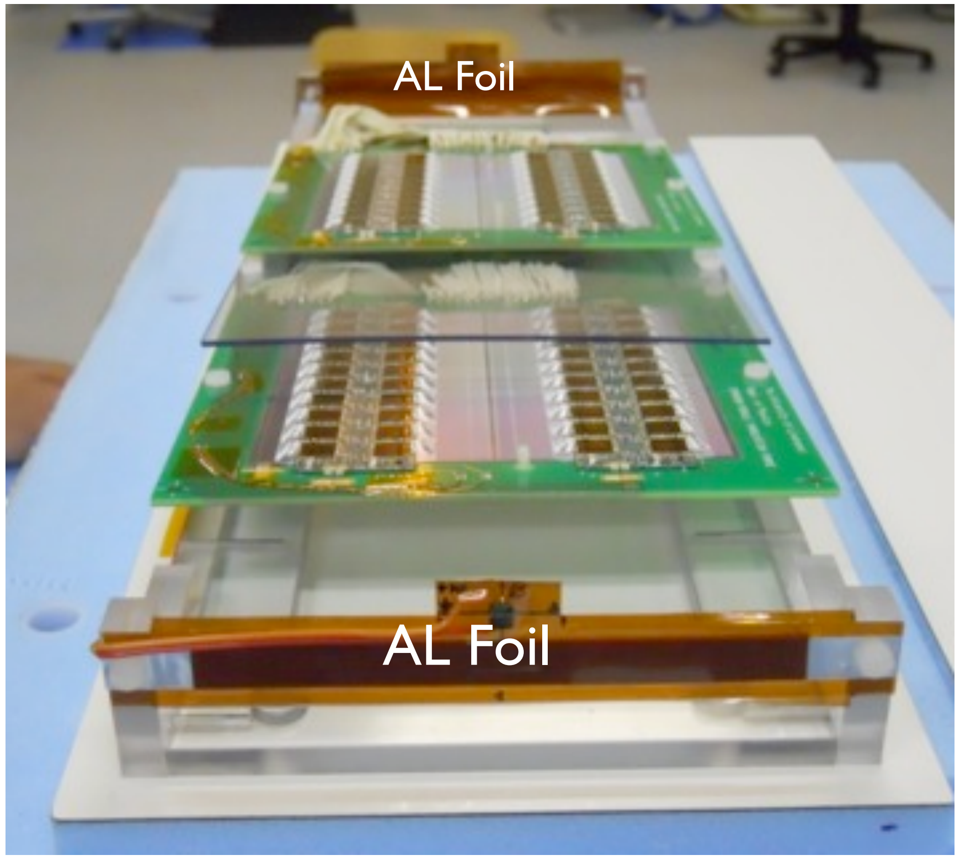




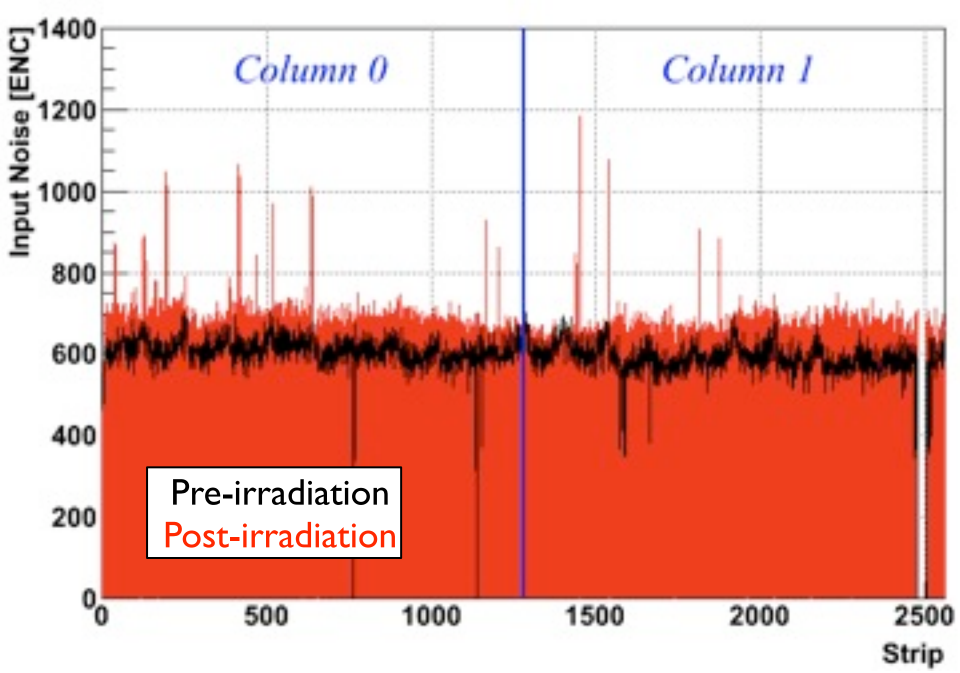
- Stave modules are tested in PCB frames
  - Cheap, flexible test bed for different power/shielding/ grounding configurations
- Parallel powering, serial powering, and DC-DC converters have all been evaluated
  - With proper grounding/shielding, all these configurations give expected noise performance

	Parallel	Serial	DC-DC
Hybrid 62	590 e^- 596 e^-	590 e^- 599 e^-	595 e^- 603 e^-
Hybrid 61	585 e^- 591 e^-	588 e^- 599 e^-	585 e^- 591 e^-

Strip Module Irradiation

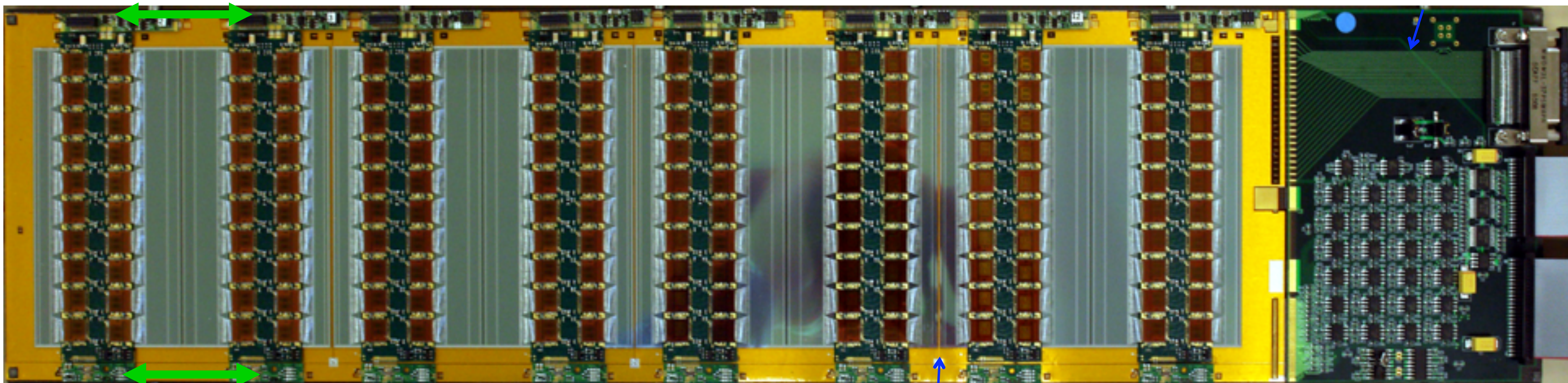


- Irradiated at CERN-PS irradiation facility
  - 24 GeV proton beam scanned over inclined modules
  - Module biased, powered, and clocked during irradiation
  - Total dose of 1.9×10^{15} n_{eq} cm^{-2} achieved
    - Max predicted fluence for barrel modules is 1.2×10^{15} n_{eq} cm^{-2}
- Sensor and module behave as expected
  - Noise increase consistent with shot noise expectations
- Rather difficult study as full devices tend to get “hot”

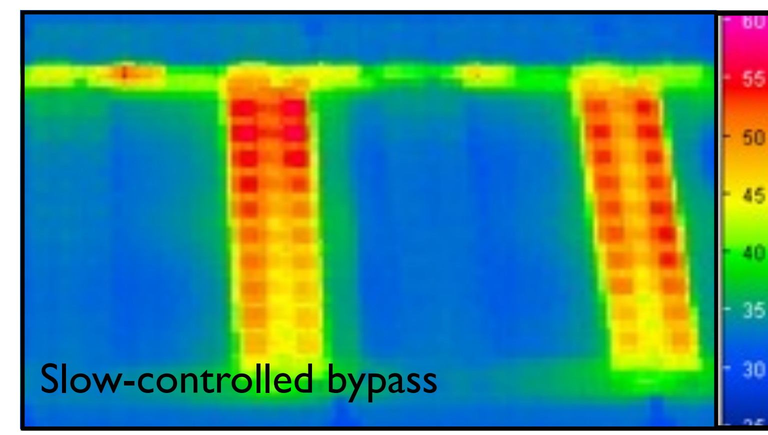


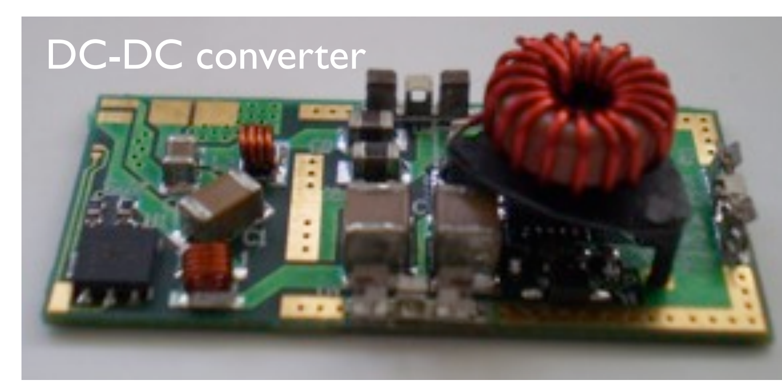
Noise	Column 0	Column 1
Pre-Irrad	610 e^-	589 e^-
Post-Irrad	675 e^-	650 e^-
Difference	65 e^-	61 e^-
Expected	670 e^-	640 e^-

Stavelets



- Shortened stave built as electrical test-bed
  - Shielding, grounding, serial and DC-DC powering, …
- First stavelet serial powered
  - Power Protection Board (PPB) has automated over-voltage protection and slow-controlled (DCS) hybrid bypassing
  - **DC-DC stavelet under construction**
- Uses Basic Control Chip (BCC) for data I/O
  - Generates 80MHz data clock from 40MHz BC clock
  - 160Mbit/s multiplexed data per hybrid

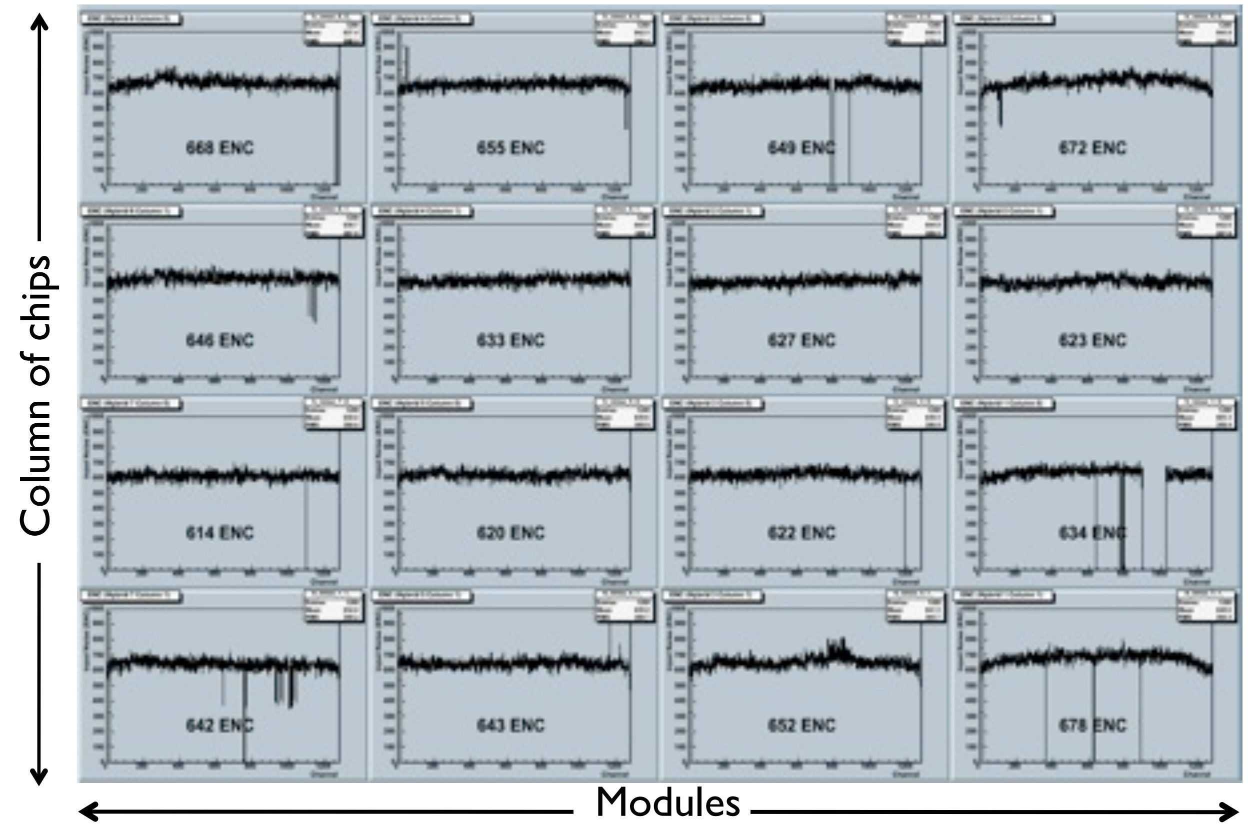


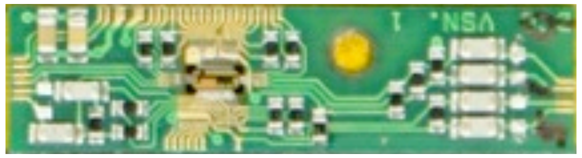


Serial Powered Stavelet Electrical Results

- Uses on-hybrid shunt control circuit
- Stavelet noise approaching single module tests
  - Roughly ~20 e^- higher
  - Bypassing hybrids does not affect noise performance
- All technologies necessary for serial powering of stave have been prototyped and shown to work (and compatible with 130 nm CMOS)
  - Constant current source, SP protection and regulation, multi-drop LVDS
    - Currently optimizing location of components, size of SP chains
- Minimal impact on material budget
  - Estimated to be ~0.03% averaged over the stave

Stavelet Noise using Serial Power

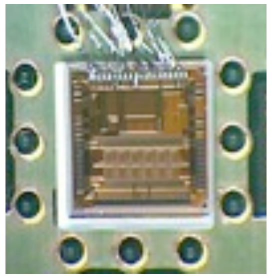




AC-coupled mLVDS

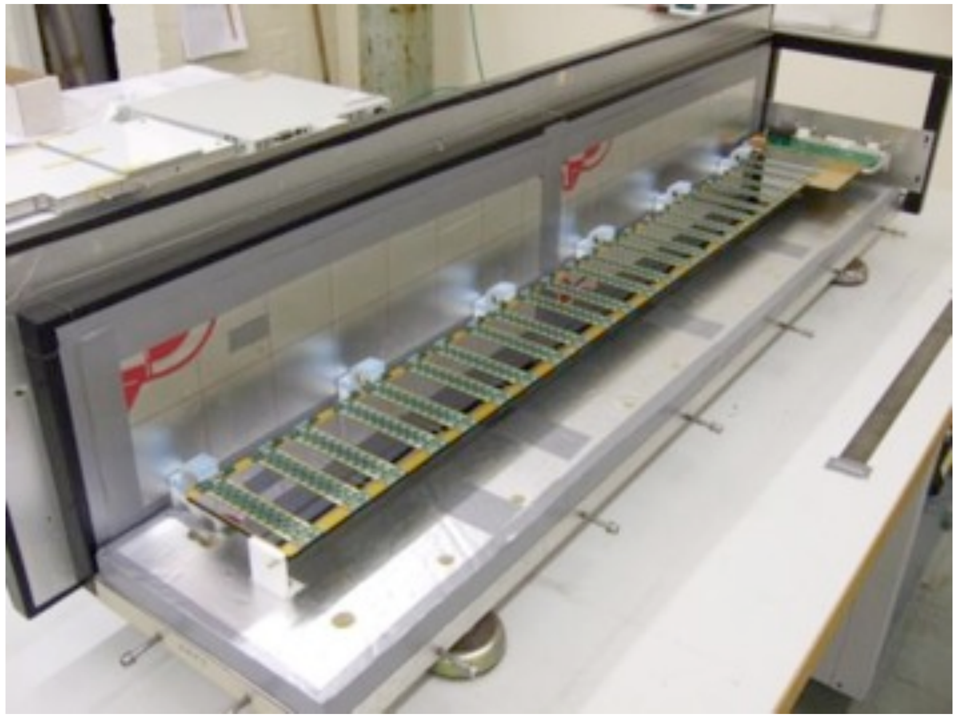
Serial Power Protection
(discrete components)

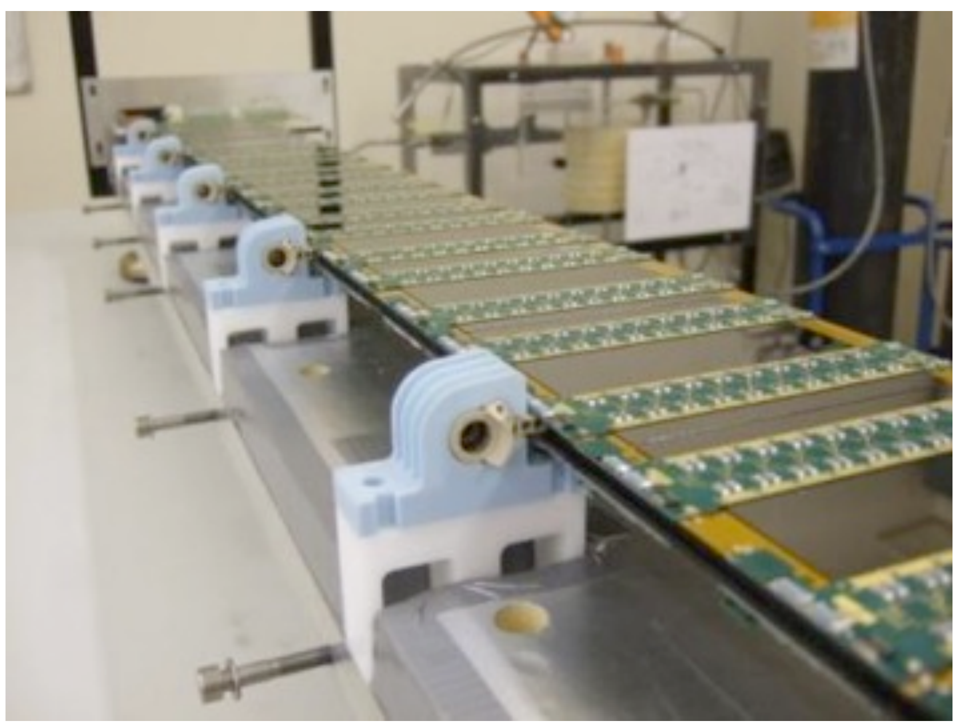
Custom Current Source



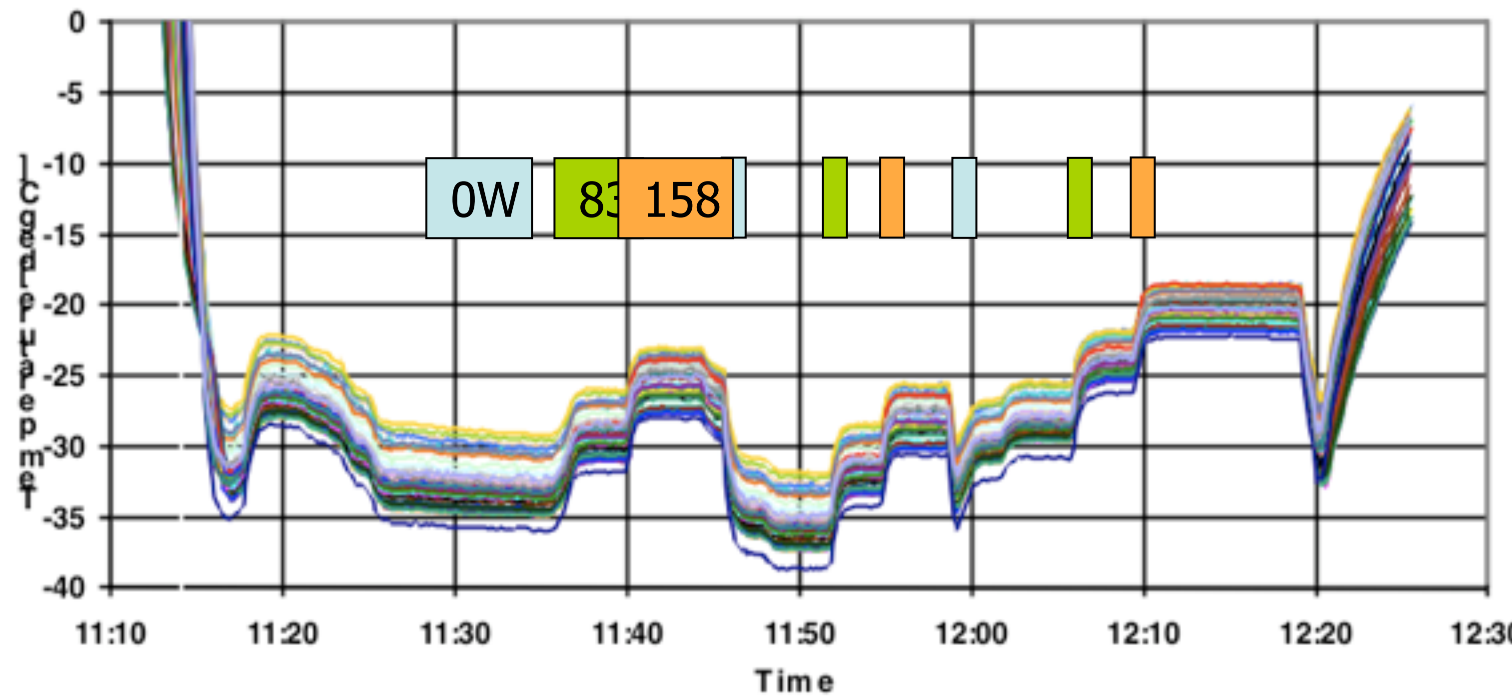
Serial Power Protection
(130 nm prototype)

Thermo-mechanical Demonstrator





Full-size demonstrator made with realistic mechanical modules, stave cores, bus cables and locking mechanism. It is cooled to -35 C° with a CO_2 blow system. During cooling from room temperature to operating temperature, deflections *<u>less than 100 µm</u>* were measured.



Thermal resistance (hybridΔT/total power):

Top: 0.0425 ± 0.0024 °C/W

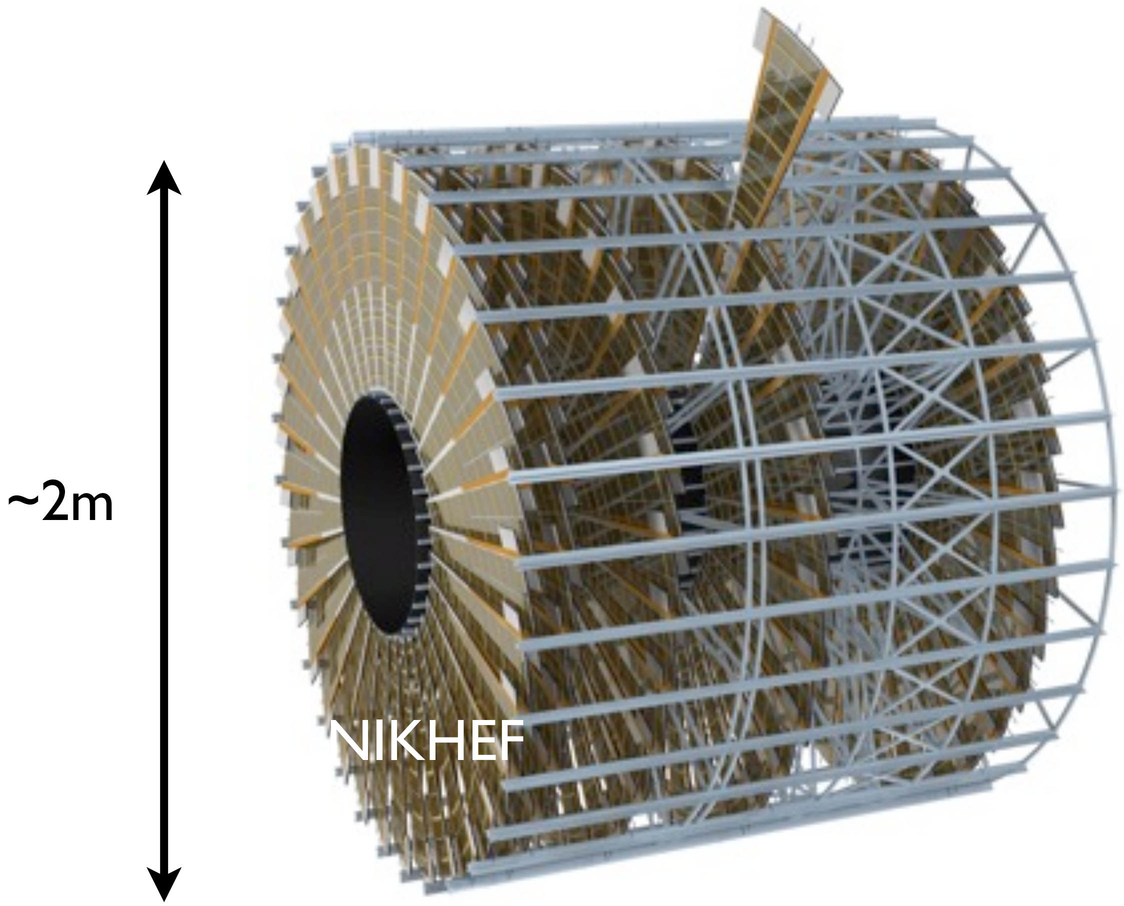
Bottom: 0.0474 ± 0.0030 °C/W

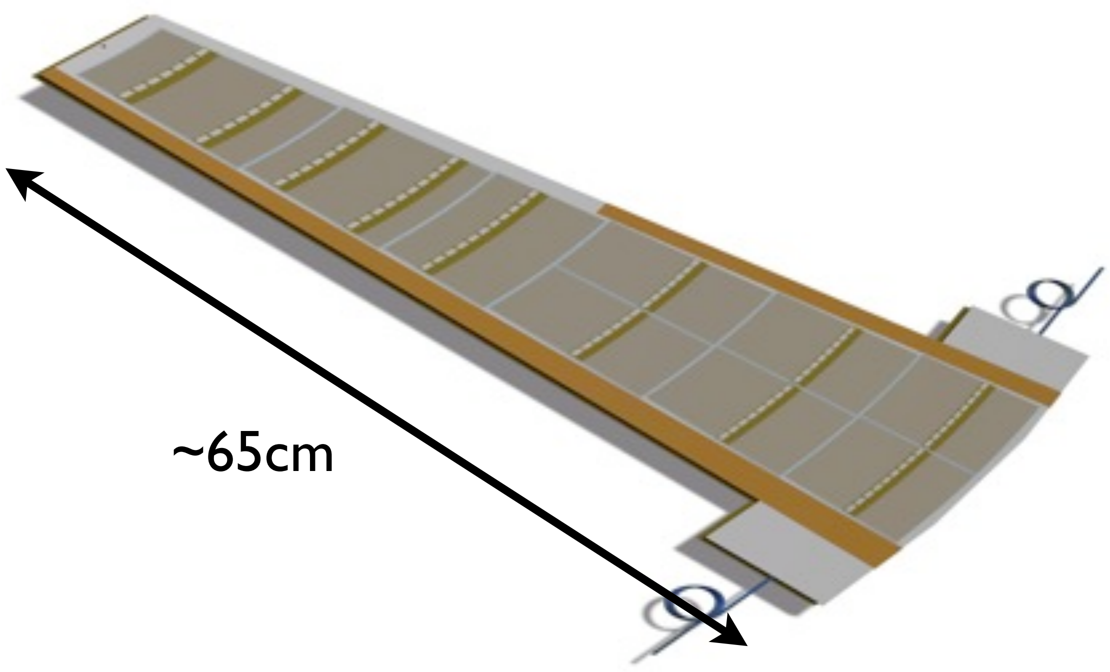
All: 0.0449 ± 0.0037 °C/W

Simulation: 0.043 °C/W

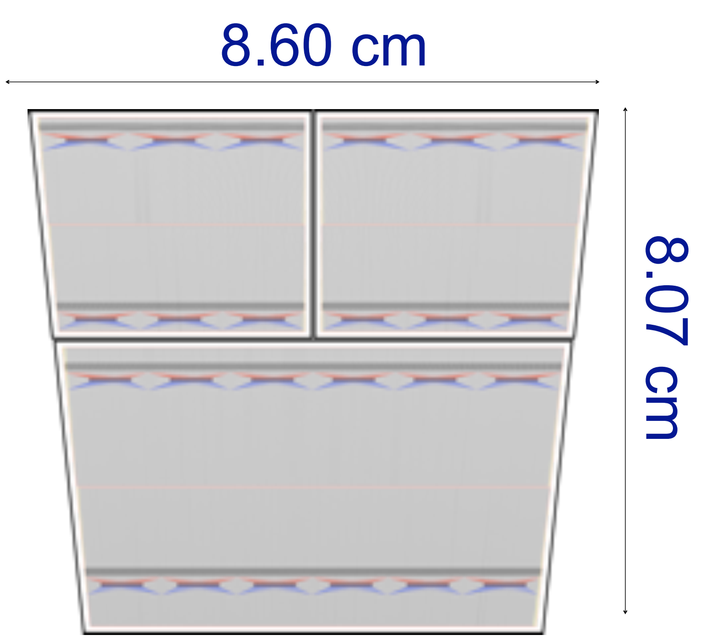
Great agreements between measurement and simulation!!

Requirements for Disc



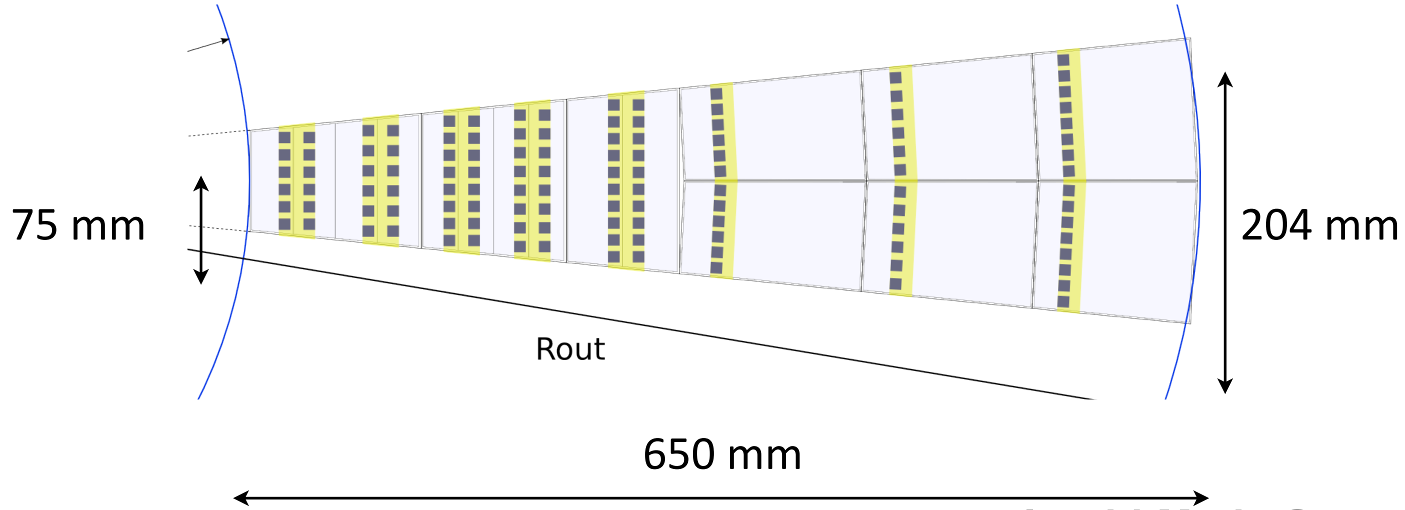


- Strips pointing to IP (phi resolution)
- Full coverage from r=336mm - 951 mm
- z position 1376mm - 2791 mm -> 5 discs
- Stereo angle +/- 20mrad
- Low material !!
- Petal seems currently the optimal design

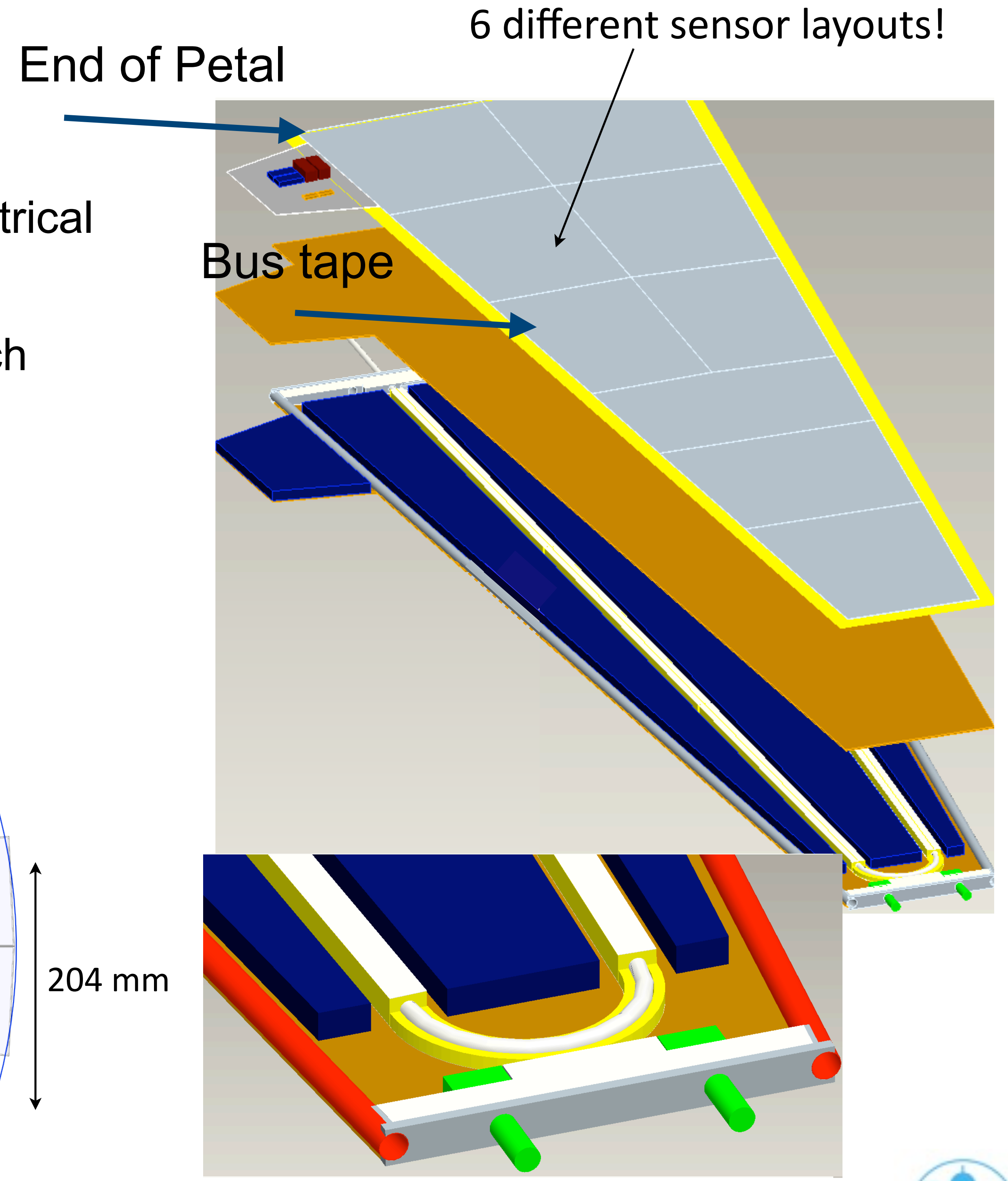


What is a petal

- **Hybrid** = capton board with FE chips (ABCNext, connection via wire bonds)
- **Module** = silicon sensor with readout hybrid (connection via wire bonds)
- **Petal** = petal core structure + cooling + electrical services (power, data, TTC) + modules:
  - 2 Carbon Facings + Honeycomb sandwich core (6mm)
  - Carbon Fibre tubes on sides
  - Independent CO_2 cooling pipe
  - Independent e- services + Bus cable
  - Control card on side
  - 2x9 modules



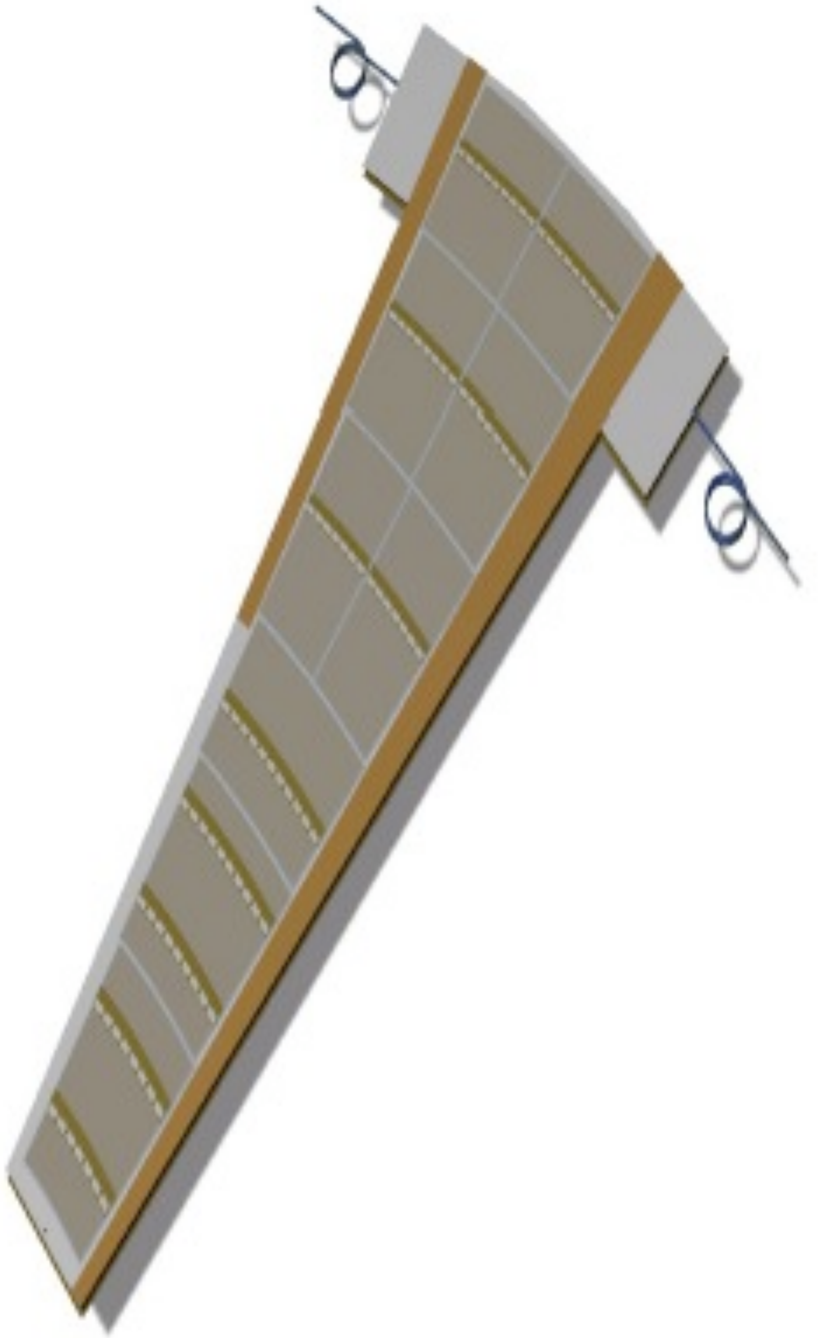
Hybrid positions and dimensions



Strip pitch etc

Sensor ring	Hybrid	Numb. chips	Pitch (micron)
1	Inner	7	78.8
1	Outer	8	78.6
2	Inner	9	78.7
2	Outer	10	78.6
3		11	78.7
4		7	74.2
5		8	76.1
6		9	76.8

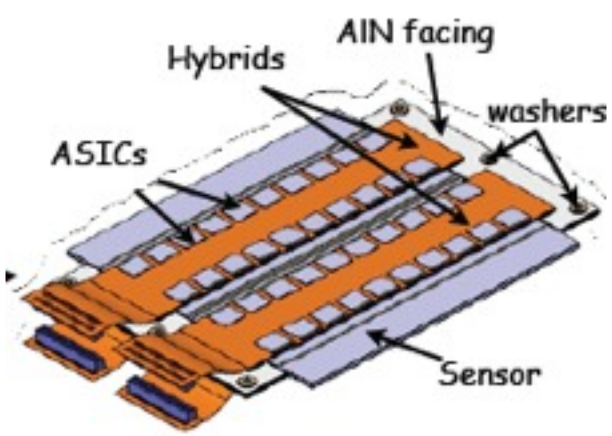
- UTOPIA layout
- In the current design we have 6 different sensor type, leading to 8-11 different hybrid designs

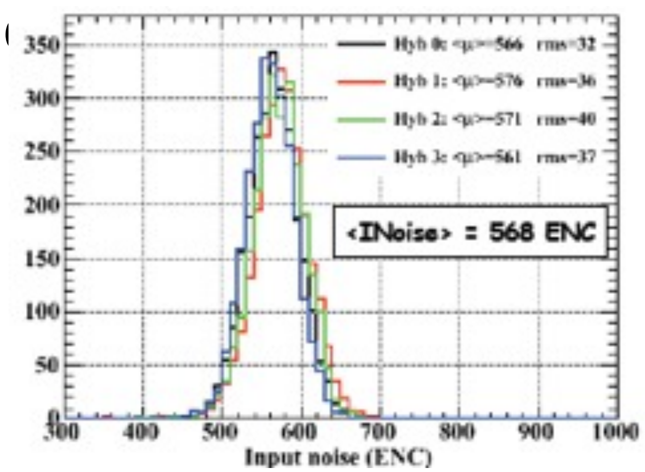


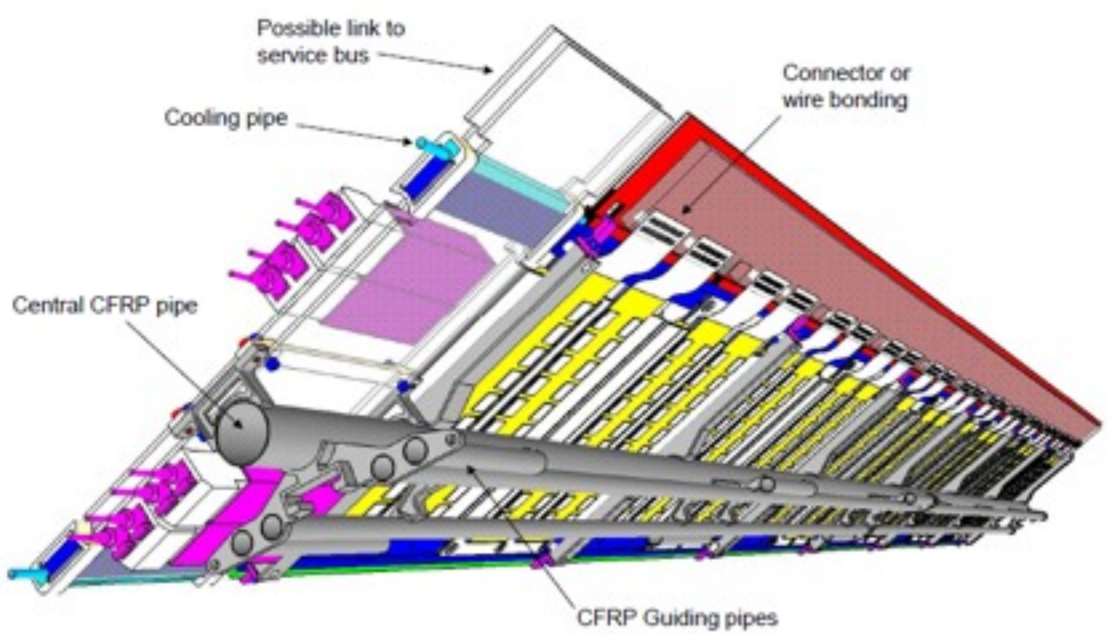
Possible petal design

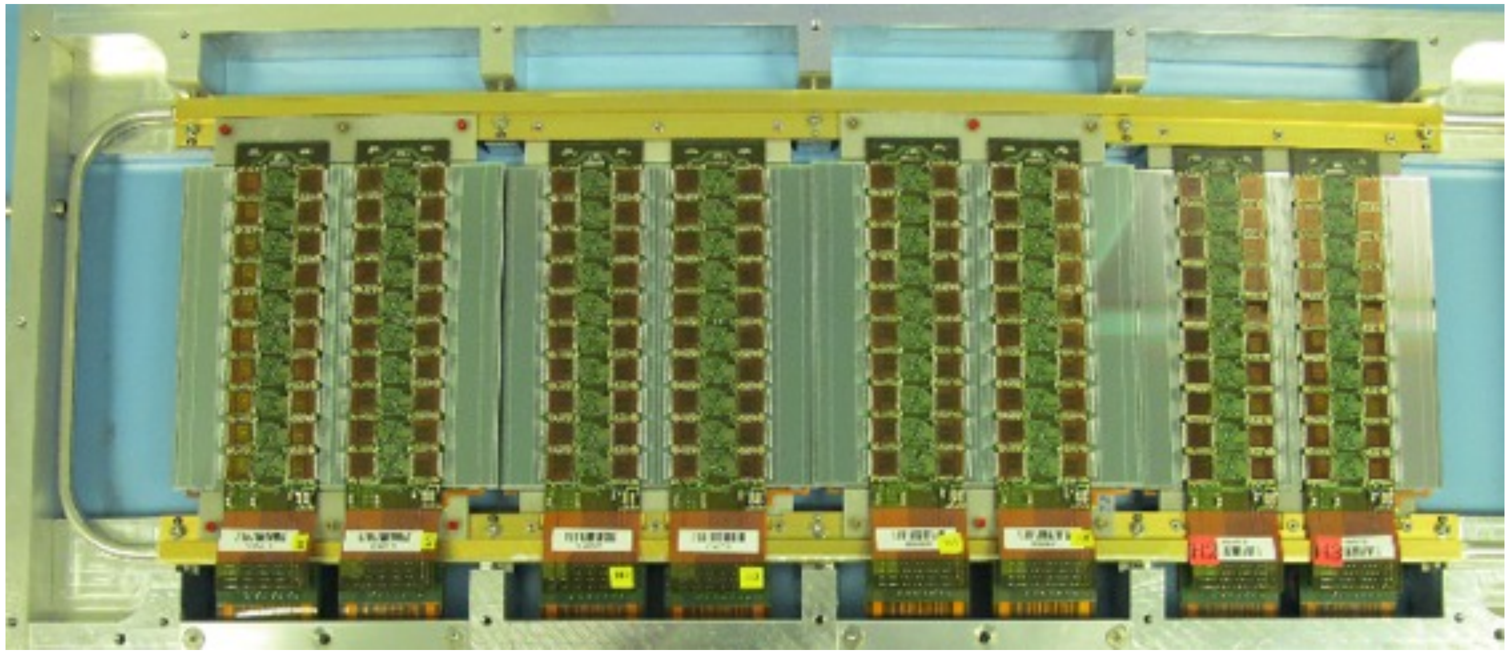
Alternative Solution: Super-Module

- Modular concept: cooling, local structure, service bus, power interface are decoupled from the modules
- Overlapping coverage in Z
- Rework – Possible up to the commissioning after integration
- Design includes carbon-carbon hybrid bridge
  - Hybrid could be also glued as for stave modules to redu[ce] material

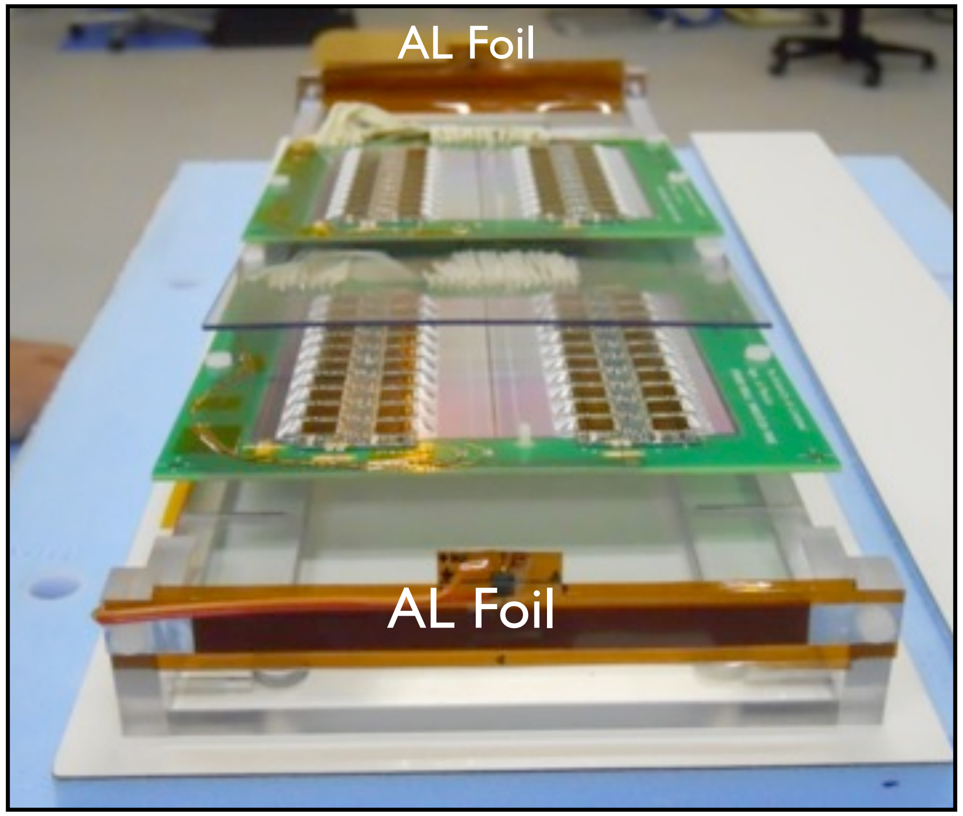






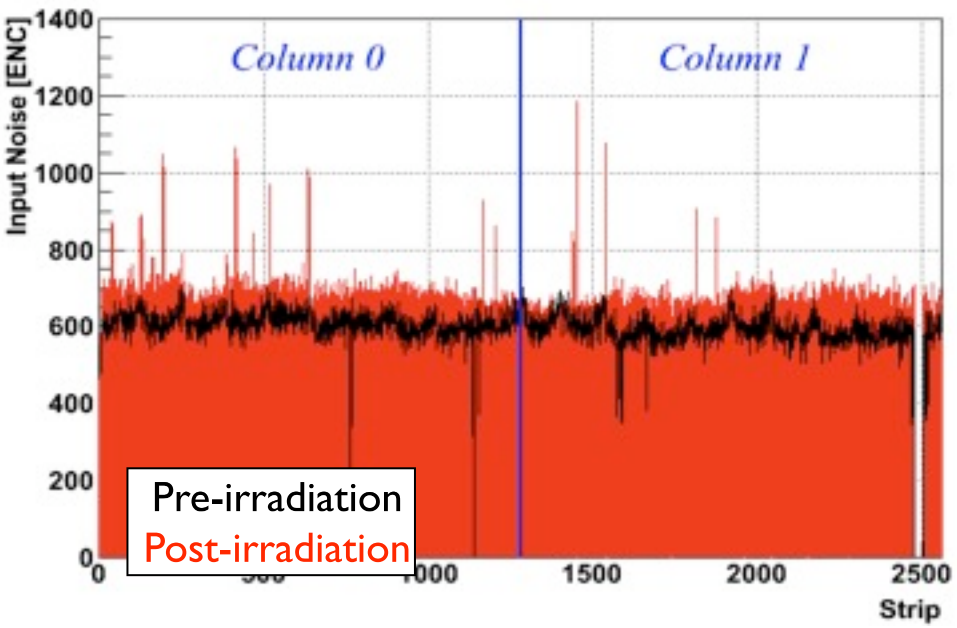


ATLAS Strip Module Irradiation



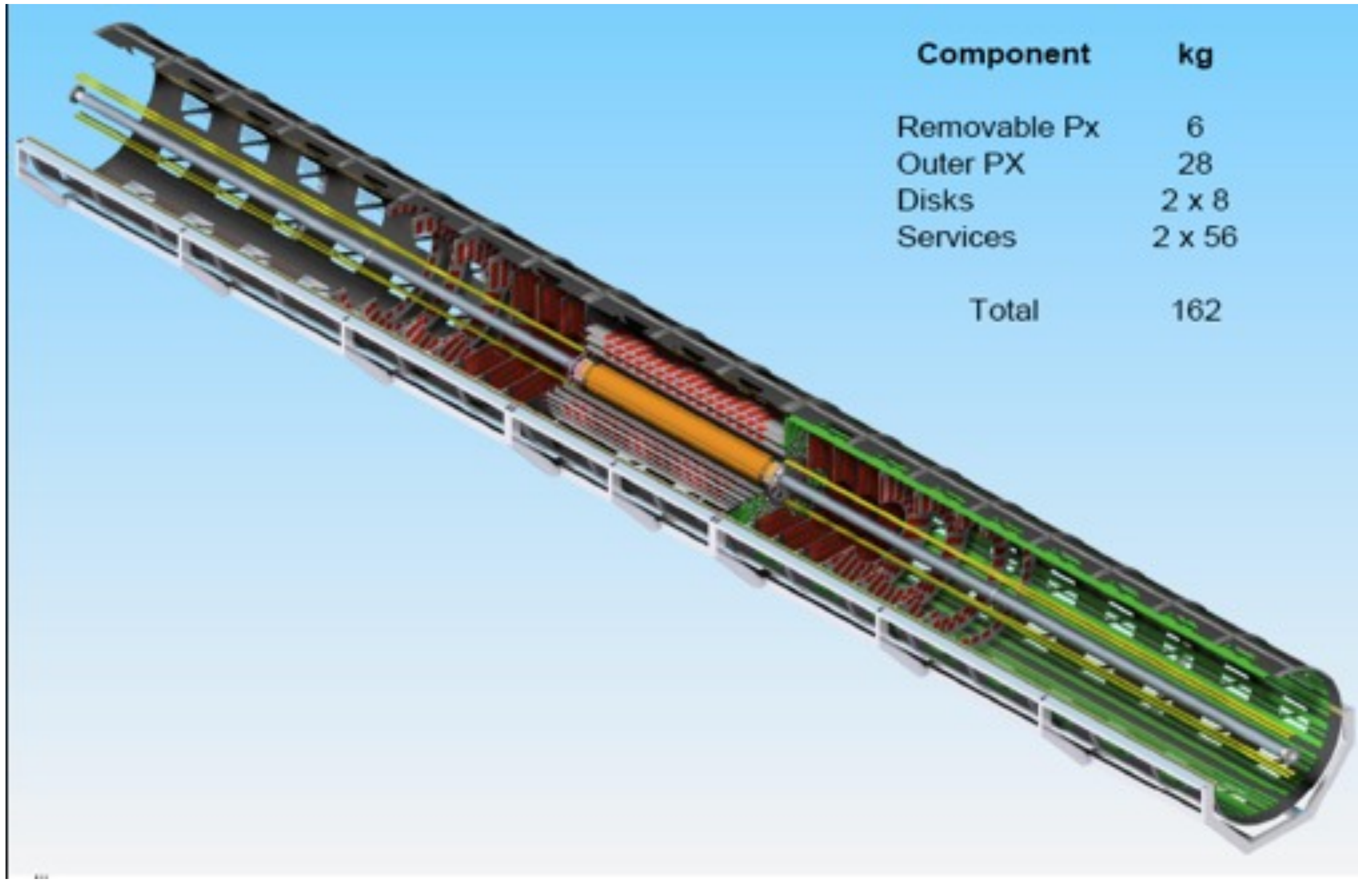
- Irradiated at CERN-PS irradiation facility
  - 24 GeV proton beam scanned over inclined modules
  - Module biased, powered, and clocked during irradiation
  - Total dose of $1.9\text{x}10^{15}$ n_{eq} cm^{-2} achieved
    - Max predicted fluence for barrel modules is $1.2\text{x}10^{15}$ n_{eq} cm^{-2}
- Sensor and module behave as expected
  - Noise increase consistent with shot noise expectations

HAMAMATSU

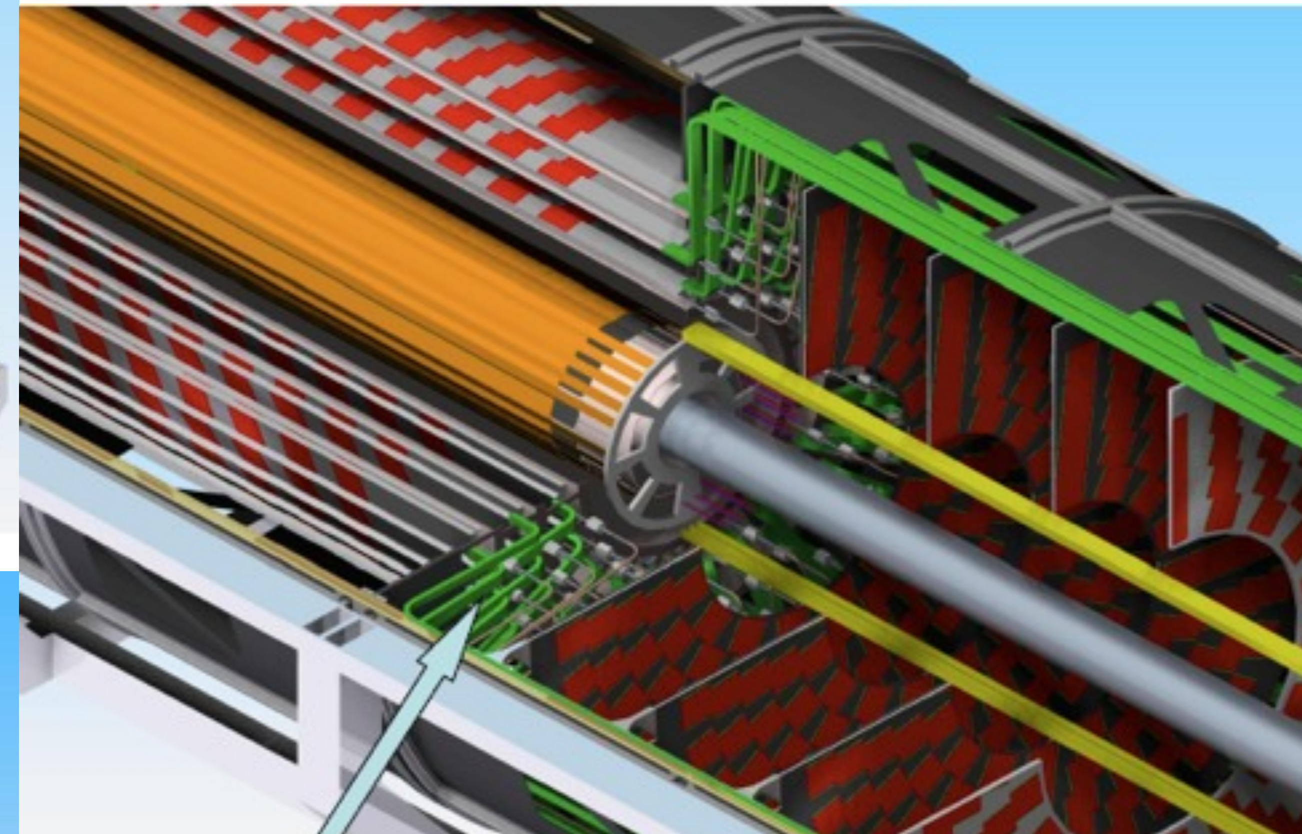


Noise	Column 0	Column 1
Pre-Irrad	610 e^-	589 e^-
Post-Irrad	675 e^-	650 e^-
Difference	65 e^-	61 e^-
Expected	670 e^-	640 e^-

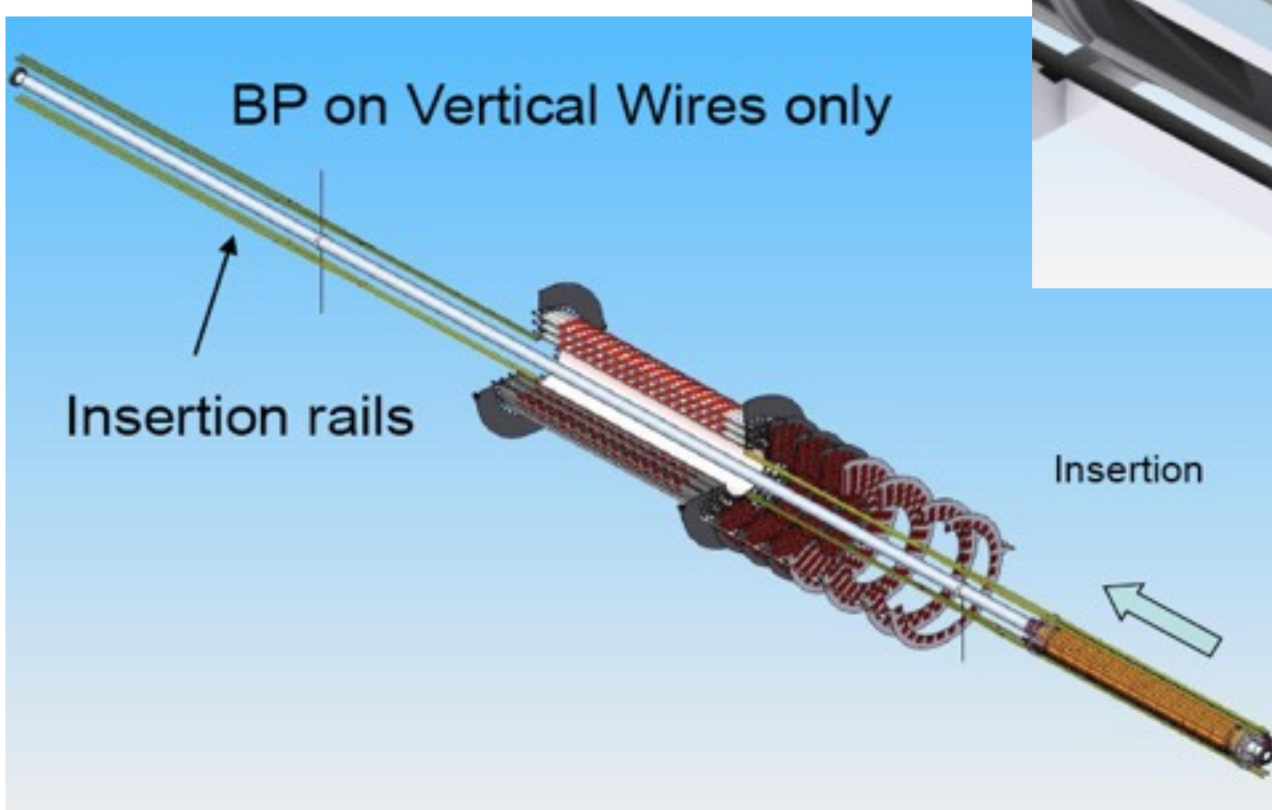
Possible Phase-II Pixel Mechanics



Independent thermal enclosure
for replacement pixel package



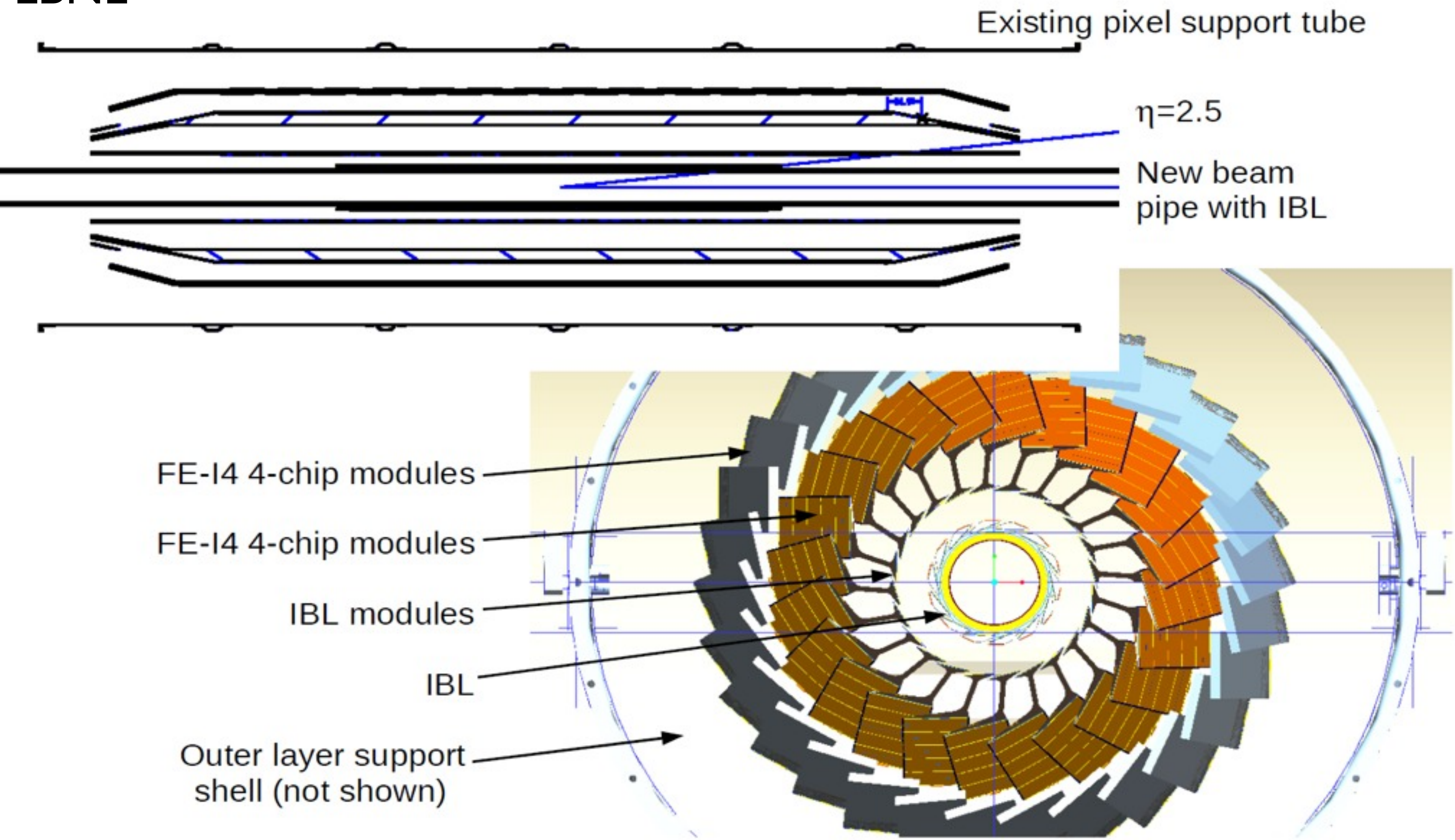
SLAC



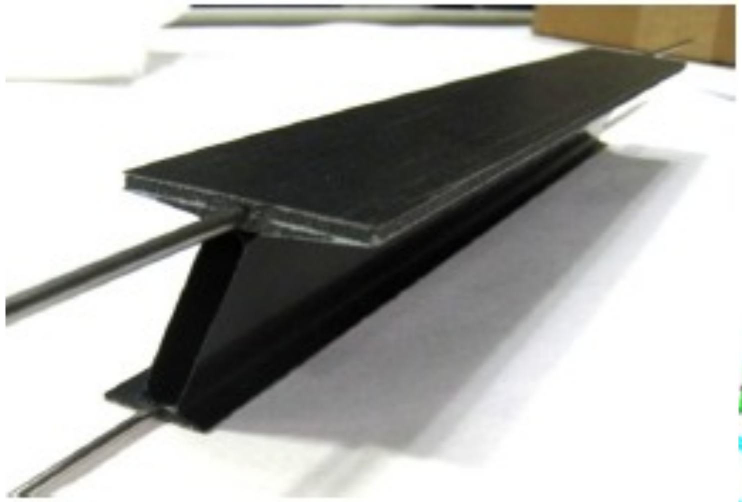
IBL remains separately insertable

Independently Installable Pixel Design

LBNL

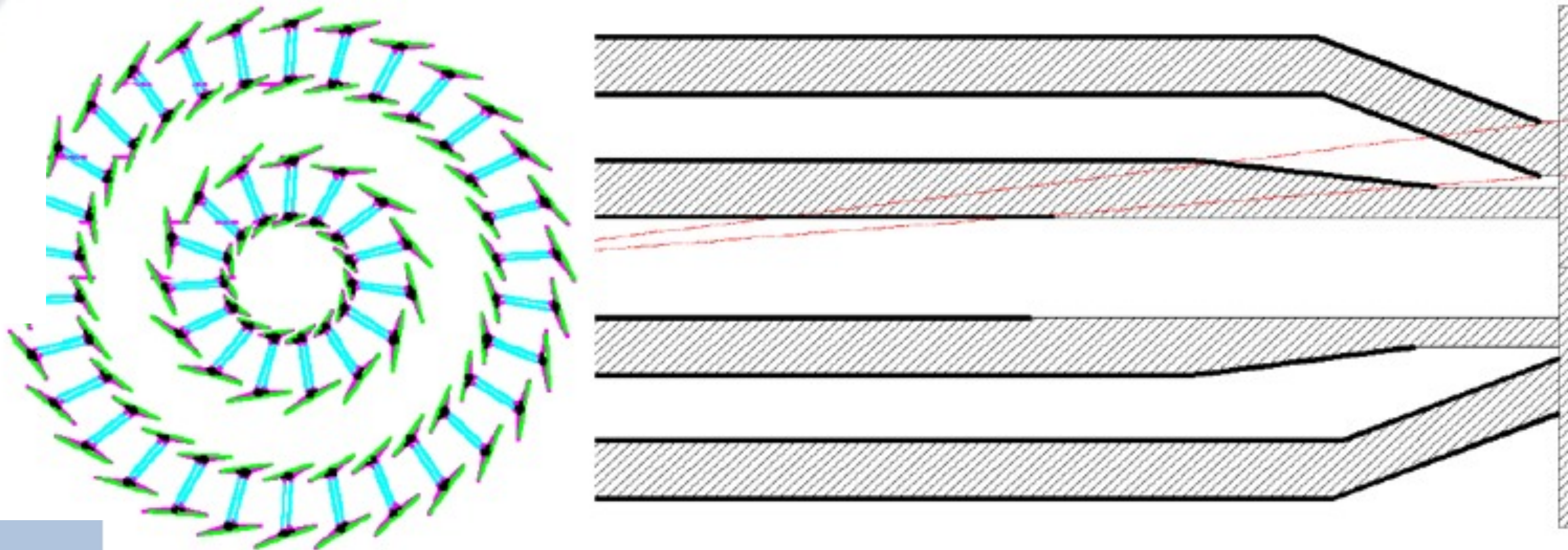


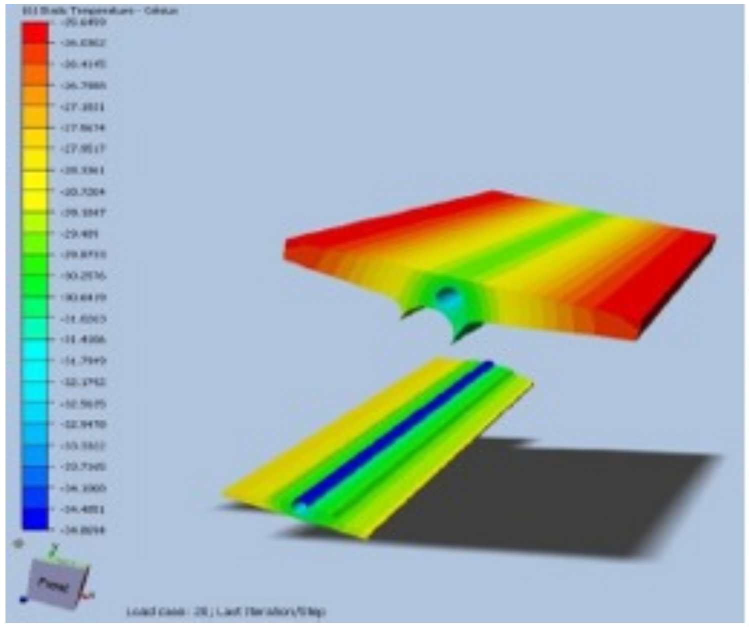
Material Reduction



I-beam prototype, LBNL 2010

LBNL



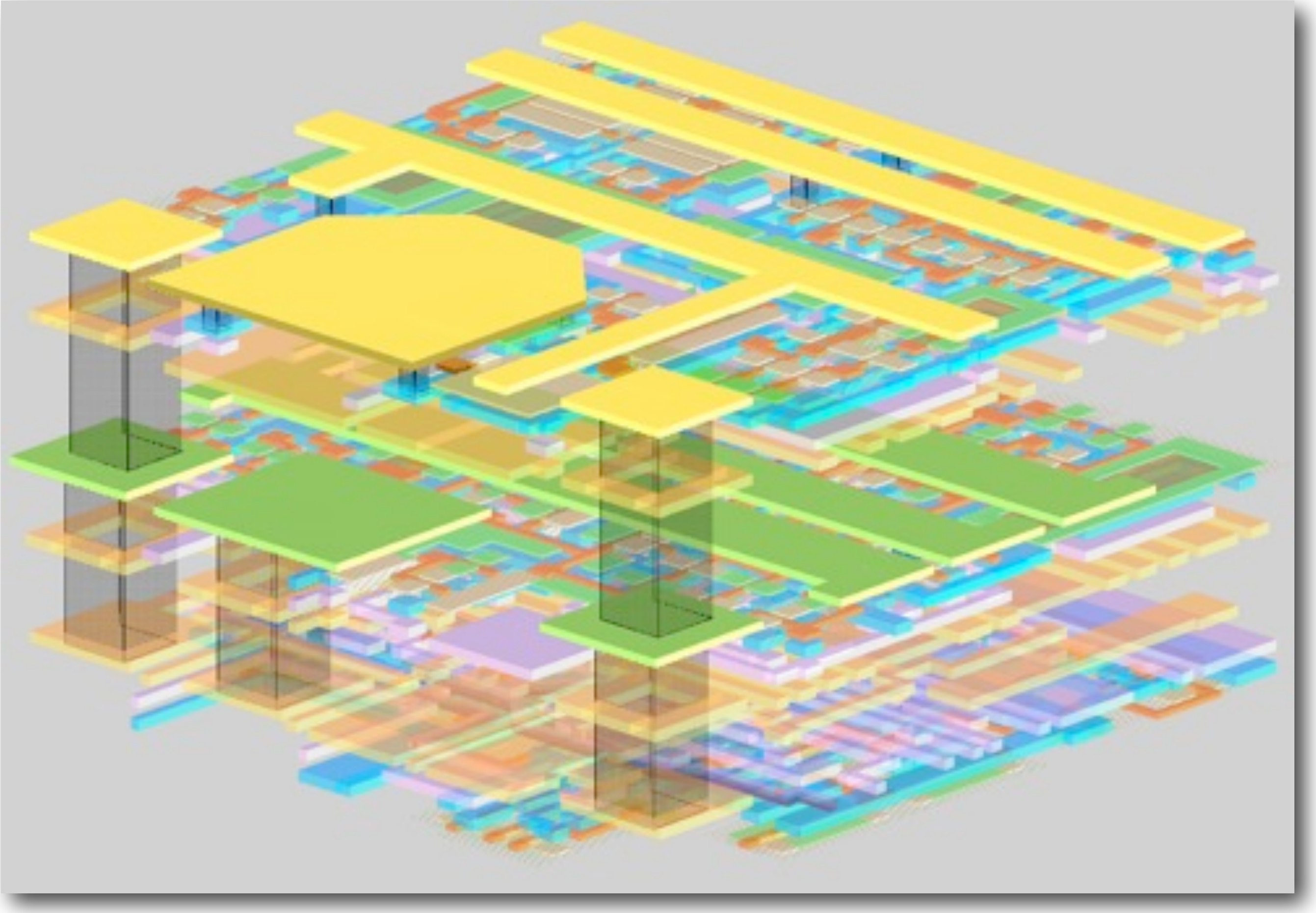


	Present detector + IBL	Double I-Beam
Number of channels	92 M	276 M
Global supports mass	8.3 kg	2.1 kg
Local supports mass	6.6 kg	5.6 kg (meas.)
Silicon mass equivalent of all mechanics	5.7 kg	2.8 kg
Sensor + chip mass	2.9 kg	4.4 kg (*)
Total silicon equivalent	8.7 kg	7.2 kg

Ultimate Interconnection: Vertical Integration

Ideal solution for reducing material and easing assembly in detector system is to integrate electronics and sensors into a single item
… if affordable

- This has been a “dream” for many years
- More complex detectors, low mass
- Liberate us from bump/wire bonding



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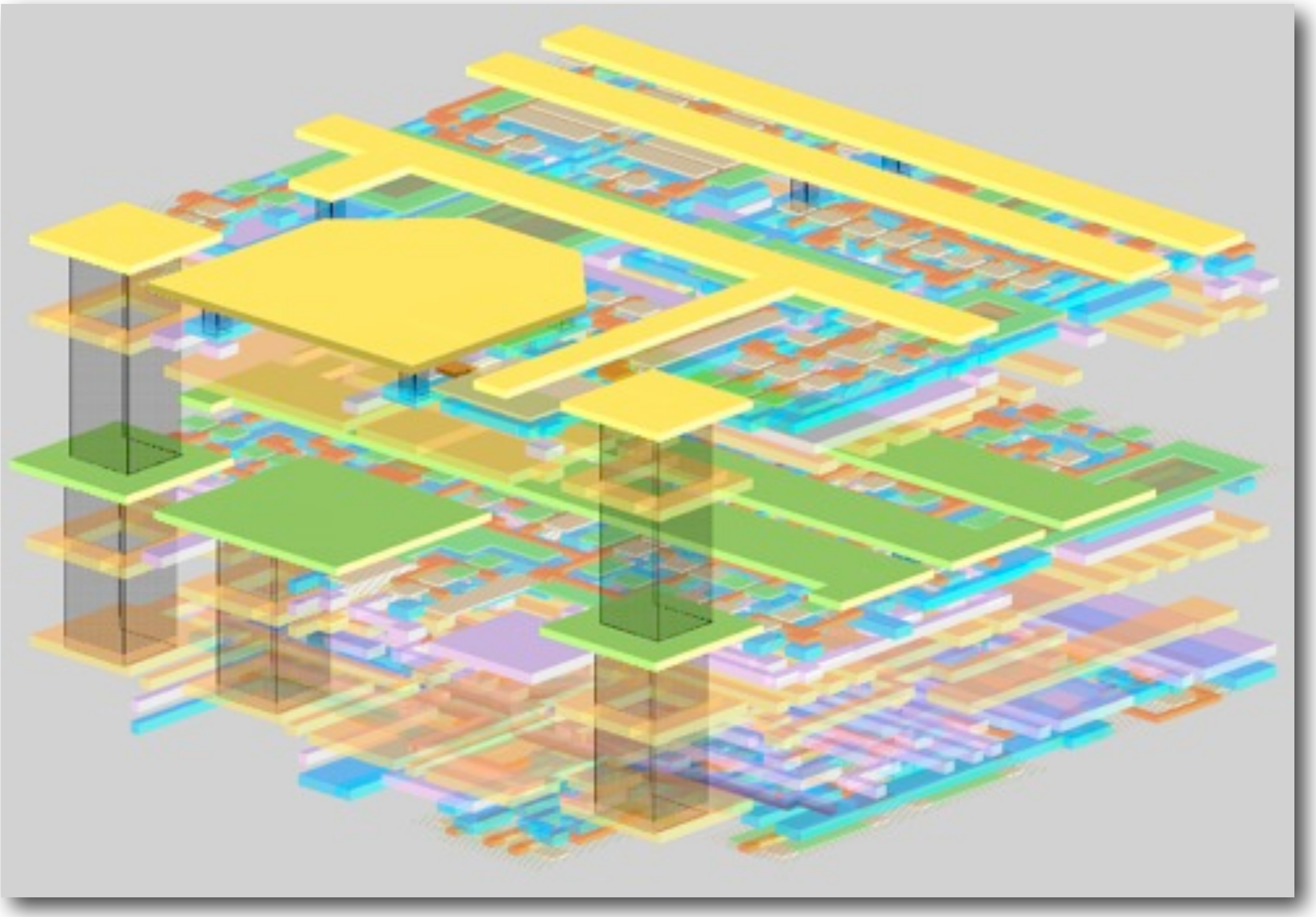

Many different aspects of these new technologies such as SLID (solid liquid inter-diffusion), TSV (through silicon vias), ICV (inter-chip vias) as well as more highly integrated concepts.

Commercial technologies becoming available for custom design:
IBM, NEC, Elpida, OKI, Tohoku, DALSA, Tezzaron, Ziptronix, Chartered, TSMC, RPI, IMEC……..

But are they all, or even, are any technologies radiation hard?

Conclusions

- The current schedule for the LHC foresees running well into the next decade to accumulate up to 3000 fb^{-1}
- In the first LHC shutdown (2013) an additional pixel layer will be installed.
- The current ATLAS Inner Detector are designed to withstand ~700 fb^{-1} -> must be replaced with an all-silicon tracker for HL-LHC operation (planned to be assembled by 2020)
- Such a High Luminosity LHC requires granularity and radiation hardness in the tracking detectors that are, again, a factor of 10 greater than before.
- Plans to go beyond this are already in hand (HE-LHC, ILC/CLIC, muon collider, as well as many intensity frontier machines) but major choices must depend on what we find in the coming years.
  - Full-size prototype planar strip detectors have already been fabricated at Hamamatsu Photonics (HPK) which meet the final specifications
  - Working baseline and alternative module prototypes have been made and shown to work after irradiation larger than the final expected fluence
- Full-size stave/super-module prototypes are planned to be finished this year with the next generation of the 130 nm ASICs for the strip tracker under design