Exploration of Graphene Synthesis and Devices via Interface Engineering

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In this talk, we will present our recent efforts on interface engineering of substrate surface for graphene synthesis and device fabrication, as well as their applications in high-quality graphene transistors and memory devices.

As a substrate surface is ubiquitously used as a supporting platform for graphene sheet formation as well as carrier transport in the active graphene layer, the surface functionalities play an important role for effectively controlling graphene growth and minimizing the interface scattering effect, as well as increasing the carrier mobility. In fact, our recent results have shown that high-quality graphene sheets can be synthesised from different solid polycyclic hydrocarbon precursors on catalytic copper/nickel surface, and high-performance graphene devices can be achieved on passivated SiO_2 surface on Si substrate with self-assembled monolayers (SAMs). Here we will discuss different interface engineering strategies in producing graphene layers, improving graphene transistor performance, and exploring new graphene devices. Two major interface systems, namely, graphene/catalytic metal system, and graphene/ octadecyltrimethoxysilane ($CH_3(CH_2)_{17}Si(OCH_3)_3$) (OTMS) SAM passivated SiO_2 system will be discussed. Large-area and high-quality graphene sheets on copper surface, high-quality OTMS SAM passivated SiO_2, and the associated mechanistic understanding as well as novel graphene devices will be presented. We believe that the ultrasmooth surface platform provided by SAM passivation will be applicable for other 2D materials for achieving high-performance device performance.

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